MOTOROLA MICROSYSTEMS

M68SDT EXORciser

Emulator for M6800 Based Systems

ISSUE A

M68SDT EXORciser
Emulator for M6800 Based Systems

The EXORciser is a modularized, expandable instrument that permits "instant breadboarding" and evaluation of any M6800-based microcomputer system. It consists of a prewired, bus-oriented chassis and power supply, together with three basic modules – an MPU Module, a Debug Module and a Baud Rate Module. These provide the basic control and interface functions of a microcomputer, and house the system development and diagnostic programs. A number of separately available, optional memory modules and additional interface modules (up to twelve) may be added, simply by plugging them into existing prewired sockets, to convert the basic system into an exact prototype of a desired end system. Thus, the EXORciser, with its built-in EXbug Firmware, enables the designer to configure, evaluate and debug his final system hardware and software using actual M6800 components.

Features

- Reduces system development time and cost
- Emulates final system architecture and performance through modular building block concept with standard M6800 components
- Permits debugging of final system design through built-in diagnostic firmware
- Facilitates program development using separately available Resident Software

EXORciser Options

Basic Models:

M68SDTT1	110 Volt Table Top EXORciser
M68SDTT2	220 Volt Table Top EXORciser
M68SDTTU1	110 Volt Table Top EXORciser with USE
M68SDTTU2	220 Volt Table Top EXORciser with USE
(Dimensions:	19.25 x 17.5 x 7, W x D x H)
MEX68RK	Rack Mounted Conversion Kit

(Converts standard table-top model for rack mounting.)

Optional Assemblies:

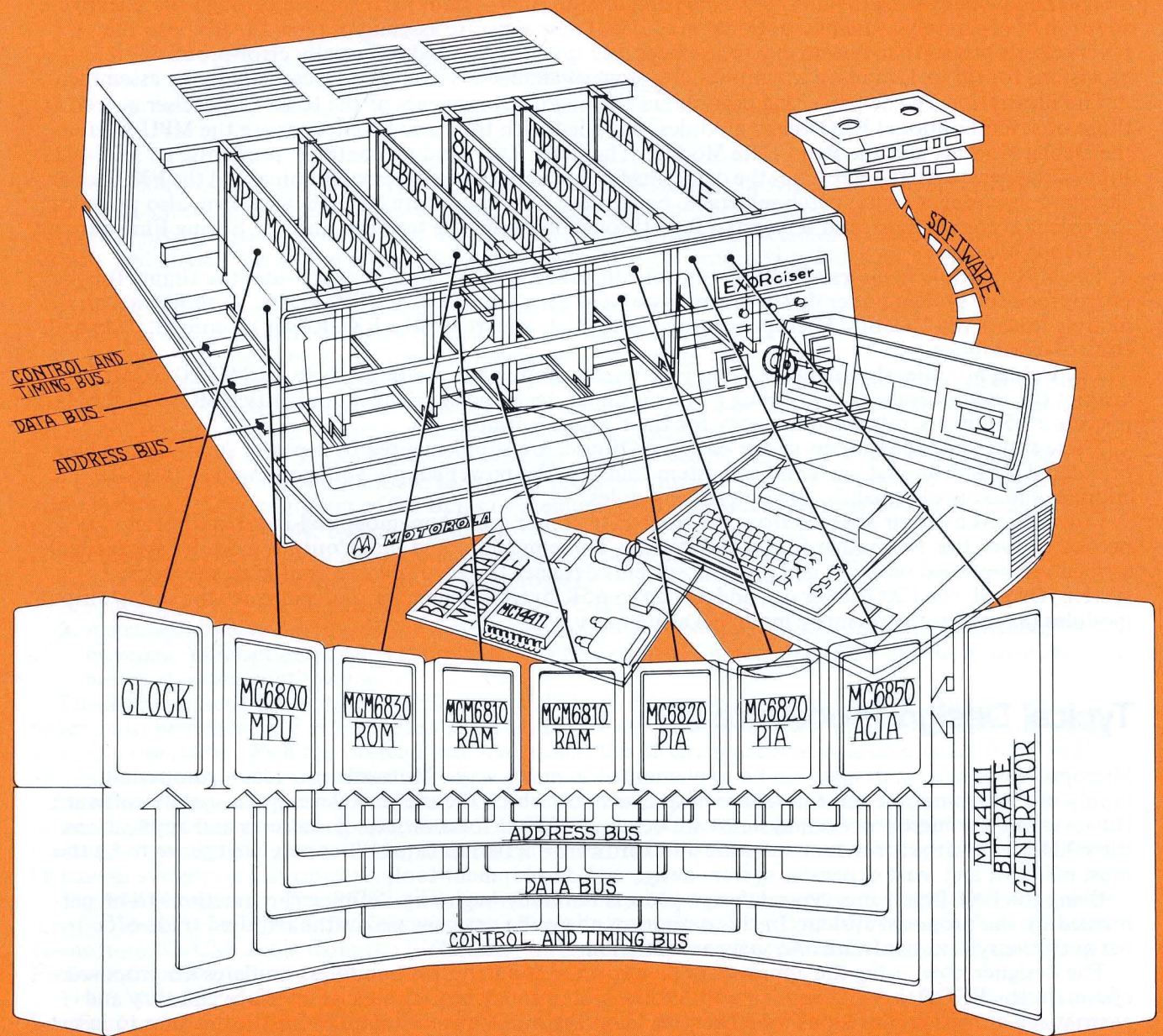
MEX6800	MPU Module (additional module)
MEX6812-1	2K Static RAM Module
MEX6815	8K Dynamic RAM Module
MEX6816-1	16K Dynamic RAM Module
MEX6820	Input/Output Module
MEX6850	ACIA Module
MEX68CT	MOTEST (Component Tester)
MEX68IC	Input/Output Flatribbon Interconnect Cable (Two per Input/Output Module)
MEX68PP	PROM Programmer Module
MEX68RR	EROM/RAM Module
MEX68SA	Systems Analyzer
MEX68USE	USE (User's System Evaluator)
MEX68WW	Wirewrap Module
MEX68XT	Extender Module

Support Software Programs:

M68ASMR021D	Resident Macro Assembler and Linking Loader on Diskette
M68XAE6812A	Resident Assembler/Editor on Cassette
M68XAE6812B	Resident Assembler/Editor on Paper Tape
M68XAE6812D	Resident Assembler/Editor on Diskette

EXORciser Specifications

Power Requirements	95-135/205-250 Vac 47-420 Hz 250 W
Word Size	
Data	8 Bits
Address	16 Bits
Instruction	8, 16, and 24 Bits
Memory Capability	65,536 bytes (maximum)
Instructions	72, variable length
Clock Cycle Time	Selectable: 1 μs crystal control clock or provisions for an external clock between 1 μs and 10 μs.
Interrupt	Maskable real-time
Data Terminal Interface Characteristics	
Baud Rates (Switch Selectable)	110, 150, 300, 600, 1200, 2400, 4800 and 9600
Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
Reader Control Signal	Control signal for TTY devices modified for external control
Operating Temperature	0-55°C


MPU MODULE
2K STATIC RAM MODULE
DEBUG MODULE
8K DYNAMIC RAM MODULE
INPUT/OUTPUT MODULE
ACIA MODULE
SOFTWARE
EXORciser
CONTROL AND TIMING BUS
DATA BUS
ADDRESS BUS
MOTOROLA
BAUD RATE MODULE
MC14411
CLOCK
MC6800 MPU
MCM6830 ROM
MCM6810 RAM
MCM6810 RAM
MC6820 PIA
MC6820 PIA
MC6850 ACIA
MC14411 BIT RATE GENERATOR
ADDRESS BUS
DATA BUS
CONTROL AND TIMING BUS

The M68SDT EXORciser

Description and Operation

The basic EXORciser contains the common ingredients of a microcomputer and offers the system designer a low-cost, versatile means of achieving unique final-system performance through the selective addition of separately available, optional modules. These separate assemblies plug directly into the EXORciser's bus so that system expansion becomes quick, easy, and essentially error-proof. With provisions for up to 12 add-on assemblies, a system of almost any complexity can rapidly be assembled.

The illustration on the preceding page shows the major components of the basic EXORciser as well as those of several optional EXORciser modules. Supplied with the basic EXORciser are the MPU Module, the Debug Module, and the Baud Rate Module. The Baud Rate Module contains, primarily, an MC14411 Bit Rate Generator that determines the data transfer rate between an external terminal and the EXORciser. The module supplies eight switch selectable baud rates. The Baud Rate Module, as shown, also provides the terminal connections, and serves as a feed-through between the terminal and the EXbug Firmware on the Debug Module.

The MPU Module includes a built-in, crystal-controlled 1 MHZ clock that provides the timing for the microprocessor system under development, as well as for the rest of the EXORciser. In addition, this module houses the MC6800 Microprocessing Unit which imparts to the EXORciser its computation and control capabilities.

The Debug Module, through its EXbug Firmware stored in the module's three MCM6830 ROMs, enables the user to evaluate and debug a system under development. The module's two MC6810 RAMs provide a 256 byte scratch-pad memory for the EXbug routines.

These functional subsystems of the basic EXORciser are supplemented by a power supply and a bus-oriented distribution system. This bus system transfers the power supply voltage as well as the data, address, and control signals to the optional modules.

Conspicuous by their absence from the basic EXORciser are the memory and input/output modules needed to turn this tool into a functional system. These memory and input/output modules are available as separate, optional modules and give the systems designer the flexibility to configure any desired system. Overall, the EXORciser can address up to 65K bytes of memory, and addresses the input/output modules (as well as the memory modules) as memory.

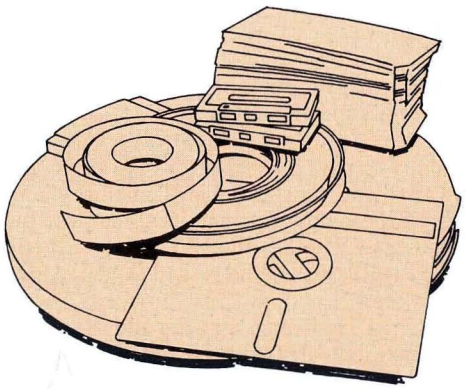
Typical Design Procedure

Microprocessor system designs can be implemented in many ways. Motorola provides a compatible family of host-computer and time-share programs upon which the user can develop his system software. However, where microprocessor systems are being developed for a variety of end uses and applications, the EXORciser with its resident software and hardware emulation capabilities may well prove to be the most efficient and least expensive system design and development tool.

Using the EXORciser in a typical design process normally begins by defining the functions to be performed by the proposed system. In this definition phase the designer makes the required trade-offs between the system hardware and software functions.

The designer now, using the appropriate memory and input/output modules, emulates his proposed system in the EXORciser. Recognizing that some systems may require special interface circuitry and customized circuitry, provisions have been made on the input/output modules for the designer to insert 14, 16 and 24 pin wirewrap sockets and construct the special interface circuitry. Also the designer can construct any customized circuitry on the Wirewrap Module.

The terminal, as illustrated, provides the means for communications between the designer and EXORciser. This can be done by means of the terminal keyboard, from paper tape, or from a cassette associated with the particular terminal in use.



The M6800 resident software, when loaded into the EXORciser, provides the designer with a powerful tool on which to develop his software. Using the capabilities of the M6800 Resident Editor, the designer enters a source program either via the terminal keyboard or from the selected medium. The user now can modify and change his source program as required to meet his proposed systems requirements. This includes:

Printing out all or any part of the program for detailed examination;
Changing any characters or string of characters in the source program;
Deleting or adding instruction lines or characters anywhere in the program.

At the end of the editing process, the Resident Editor will provide a source program that may be stored on paper tape, cassette, or diskette. This source program may be used in subsequent assembly operations on any of the compatible Motorola assemblers and cross assemblers.

The EXORciser's M6800 Co-Resident Assembler or the Resident Macro Assembler and Linking Loader can be used to automatically translate the source program into an object program. The Co-Resident Assembler requires a minimum of 8K bytes of memory while the Macro Assembler and Linking Loader requires a minimum of 14K bytes of memory.

The resultant Object Program is available from the EXORciser in three forms.

1. A printed assembly listing of the source program.
2. An Object Program on paper tape, cassette, or diskette.
3. A machine file, consisting of the machine-coded program stored directly into the EXORciser memory. This option permits the program to be executed immediately after assembly with no need for subsequent loading.

The Macro Assembler in its assembly process allows the assignment of the memory addresses of a program to be relocatable and assigned when loaded by the Linking Loader rather than fixed during the assembly operation. With the Co-Resident Assembler, the program address assignments are fixed and absolute in the assembly operation.

Once the designer has configured the EXORciser to emulate his hardware and has developed his programs, he is ready to debug his system. The EXORciser, with its EXbug system development Firmware, permits the user to debug both his system hardware and his system software as required until he has his system up and operating.

The EXORciser with its USE (User System Evaluator) option can be used to test and evaluate equipment external to its chassis. By removing the MC6800 Microprocessing Unit from the user's system and connecting the USE cable from the EXORciser into the MPU's socket, the EXORciser with its EXbug Firmware can be used to debug and troubleshoot microprocessor systems.

The EXORciser also can be used as a production tool. An EXORciser equipped with USE can be used in a final test area for testing the user's production system. With MOTEST, our component tester, the EXORciser also can be used to test the M6800 family of parts.

EXORciser Bus Signals

The EXORciser bus interfaces the MPU Module with other modules being used in the EXORciser. This bus permits the EXORciser to be configured to meet a user's specific application.

Data Bus (D0-D7) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers on the modules are three-state logic devices.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers.

Read/Write (R/W) – This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state.

Valid Memory Address (VMA) – This line, when high. indicates that the address on the bus is valid.

Valid User's Address (VUA) – This line, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi 1$ and $\phi 2$ non-overlapping clock signals.

Phase 1 ($\phi 1$) Clock – This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.

Phase 2 ($\phi 2$) Clock – This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bus Available (BA) – The Bus Available signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the Halt line is low or the MC6800 MPU is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU Module three-state output drivers will go to their off state and other outputs to their normally inactive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

Interrupt Request (IRQ) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

Reset – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser.

Three-State Control (TSC) – This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address and Valid User's Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is initially jumpered to ground on the MPU Module.

Refresh Request (REFREQ) – This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 1$ high and, through the Refresh Grant command, instructs the initiating memory module to refresh itself.

Refresh Grant (REFGRANT) – The MPU Module, on receiving a Refresh Request input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) – This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 2$ high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level.

Halt – When this input is low, all activity in the MC6800 MPU will be halted. This input is level sensitive. In the MC6800 MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the Halt line must not occur during the last 250 ns of $\phi 1$. To insure single instruction operation, the Halt line must go high for one $\phi 1$ clock pulse.

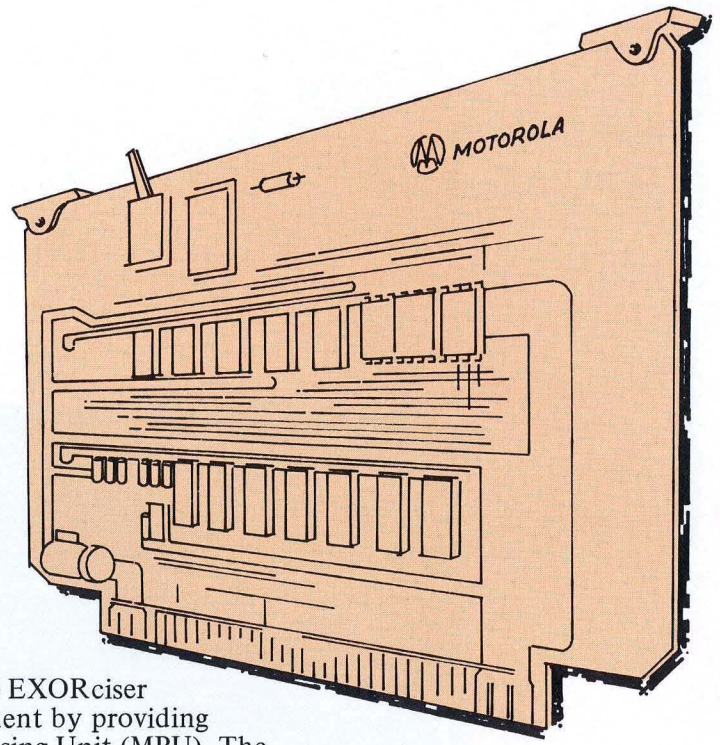
Refresh Clock (REFCLK) – This signal is generated by the dynamic memory module being used as the master refresh module. This signal is used to initiate a memory refresh operation on the dynamic modules functioning as slave refresh modules.

Stand By (STDBY) – This line is a low level during a power-fail condition and a high level during normal EXORciser operation.

Bus Control

It is possible for a module other than the MPU Module to gain control of the bus. This module would place a low level Halt on the bus and monitor the Bus Available signal. When the MPU Module completes the instruction it is performing, it generates a high level Bus Available signal. The module requesting control of the bus now must pull the Three-State Control line low, forcing the MPU Module address bus drivers to their high-impedance state. The requesting module now has control of the EXORciser bus until it elects to relinquish control.

MEX6800 MPU Module



- Provides the MPU and clock functions for both the EXORciser Debug system and the emulated user's system
- Crystal controlled 1 MHz clock
- Provisions for an external clock
- Automatic system initialization and restart capability
- Dynamic memory refresh capability on a cycle stealing basis
- Capable of working with slow external memories

The MEX6800 MPU Module is the heart of both the EXORciser Debug system and the user's system under development by providing both the system clock and the MC6800 Microprocessing Unit (MPU). The MPU Module also automatically initiates an EXORciser restart operation when power is first applied to the EXORciser.

The clock circuit generates a crystal-controlled 1 MHz signal, but the system may be operated with an external clock at frequencies between 100 kHz and 1 MHz by means of a switch mounted on the MPU Module.

In addition to generating the basic EXORciser timing signals, the clock circuit provides the EXORciser with the capability of refreshing dynamic memories and working with slow memories. The dynamic memories are refreshed on a cycle stealing basis. In working with slow memories, the MPU Module stretches the clock pulse to give the memory sufficient time to complete its assigned operation.

Specifications

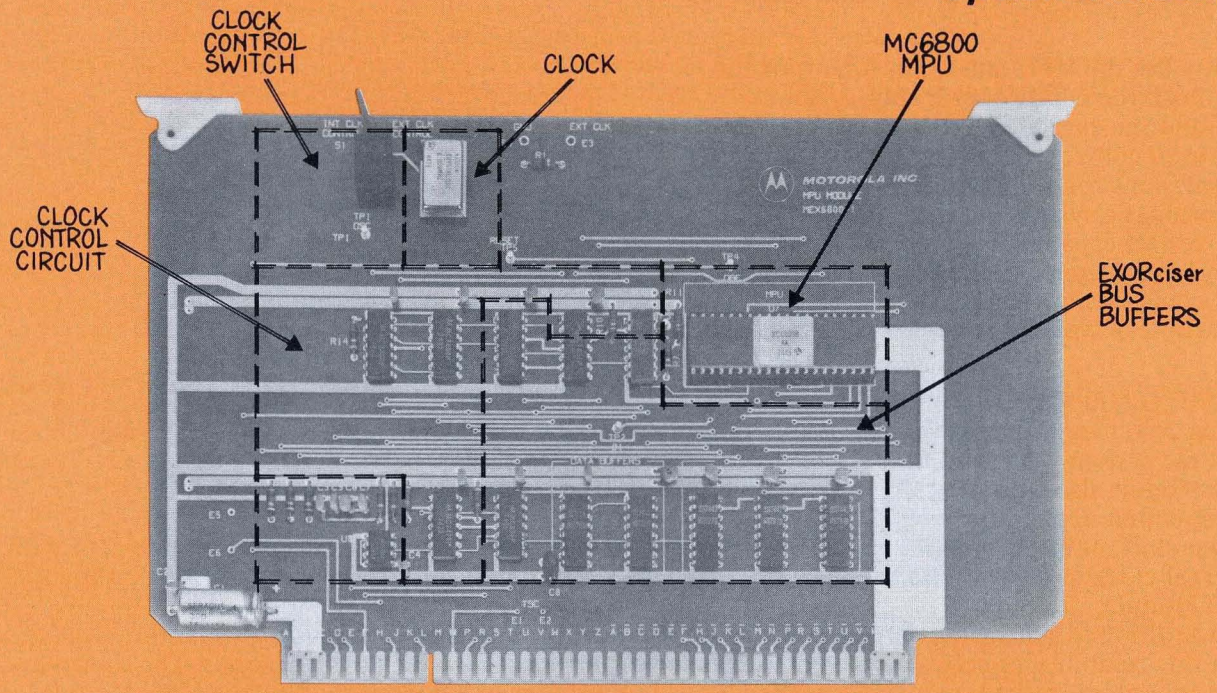
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

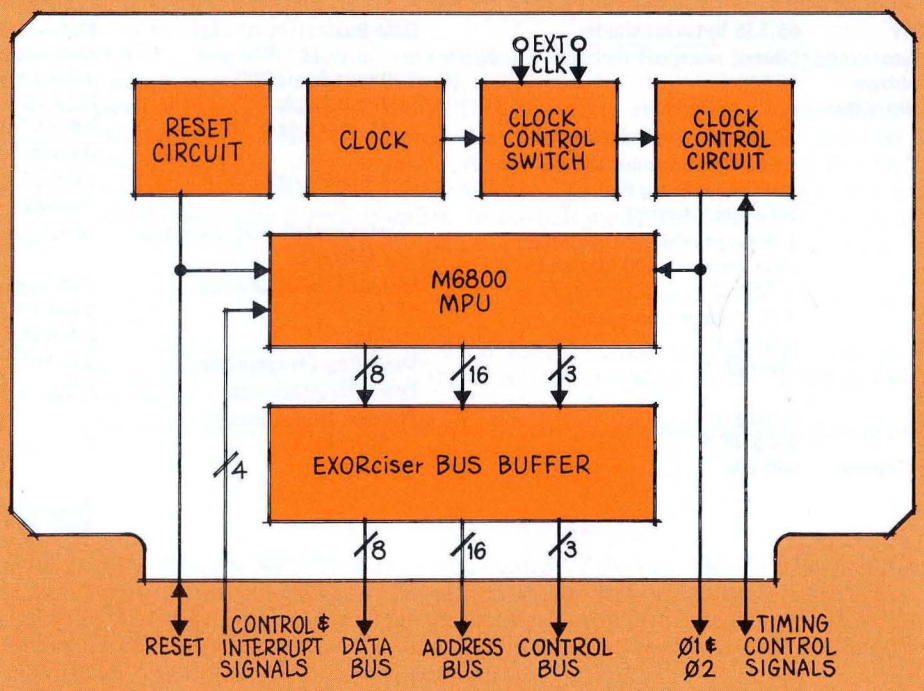
Memory Size Capability		65,536 bytes maximum
Word Size	Data	8-bits
	Address	16-bits
	Instruction	8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts Software interrupt
Clock Signal		1 MHz; provision for external clock between 100 kHz and 1 MHz
Input Control Signals		TTL Voltage Compatible
Logic "0"		0.0-0.8 V
Logic "1"		2.0-5.25 V
Address Bus and R/W		
Logic "0"		0.0-0.5 V
Logic "1"		2.4-5.25 V
Off-State Leakage Current		-40 μA

Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.8 V (-200 μA at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA at 5.25 V)
Output Logic "0"	0.0-0.5 V (40 mA at 0.5 V through a resistor to V_{CC})
Output Logic "1"	2.6-5.25 V (-10 mA at 2.6 V through a resistor to ground)
Output Off-State Leakage Current	100 μA at 2.6 V
Output Control Signals	TTL voltage compatible
Logic "0"	0.0-0.4 V
Logic "1"	2.4-5.25 V
Operating Temperature	0 to 70°C
Power Requirements	5 Vdc at 700 mA
Physical Dimensions: W x H x T	9.75 x 5.75 x 0.062 in.

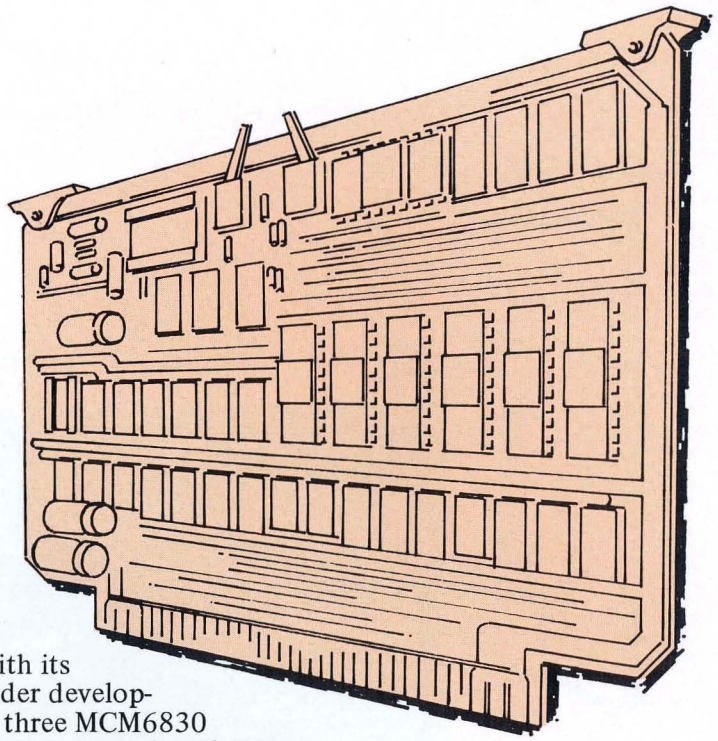
MEX6800
MPU Module

Resident
(also available as additional Optional Module)





Debug Module



- Provides EXbug system development Firmware
- Contains the special hardware to implement the EXbug functions
- Enables the user to communicate with the EXbug Firmware via a data terminal
- Interfaces EXORciser front panel switches and controls with the MPU

The Debug Module, through its EXbug Firmware and implementation hardware, provides the EXORciser with its unique capabilities to evaluate and debug a system under development. The EXbug Firmware is stored in the module's three MCM6830 ROMs with the module's two MCM6810 RAMs serving as a scratch pad memory for the EXbug routines.

Using the EXbug routines provides the designer virtually unlimited freedom in examining and debugging his proposed system hardware and software. He can, for example, search the input medium for a file, load a file into EXORciser memory, verify the contents in the EXORciser memory, print out the contents of the EXORciser memory, and record the memory contents on the selected medium. In between these input/output functions, the user can examine and, if required, change the memory contents. He can insert and remove one hardware breakpoint and up to eight software breakpoints. He also can run in real time or trace through the user's program or a selected portion of the user's program. While using these routines, the user modifies his hardware and software as required until he has his system up and running. The DISABLE switch on the module may be used to disable the EXbug routines.

The user communicates with EXbug via an external terminal working in conjunction with the Baud Rate Module and the Debug Module. The STOP-ON-ADDRESS/SYNC ENABLE switch on the Debug Module is used to generate a sync pulse at a pre-selected address or to enable the hardware breakpoint function.

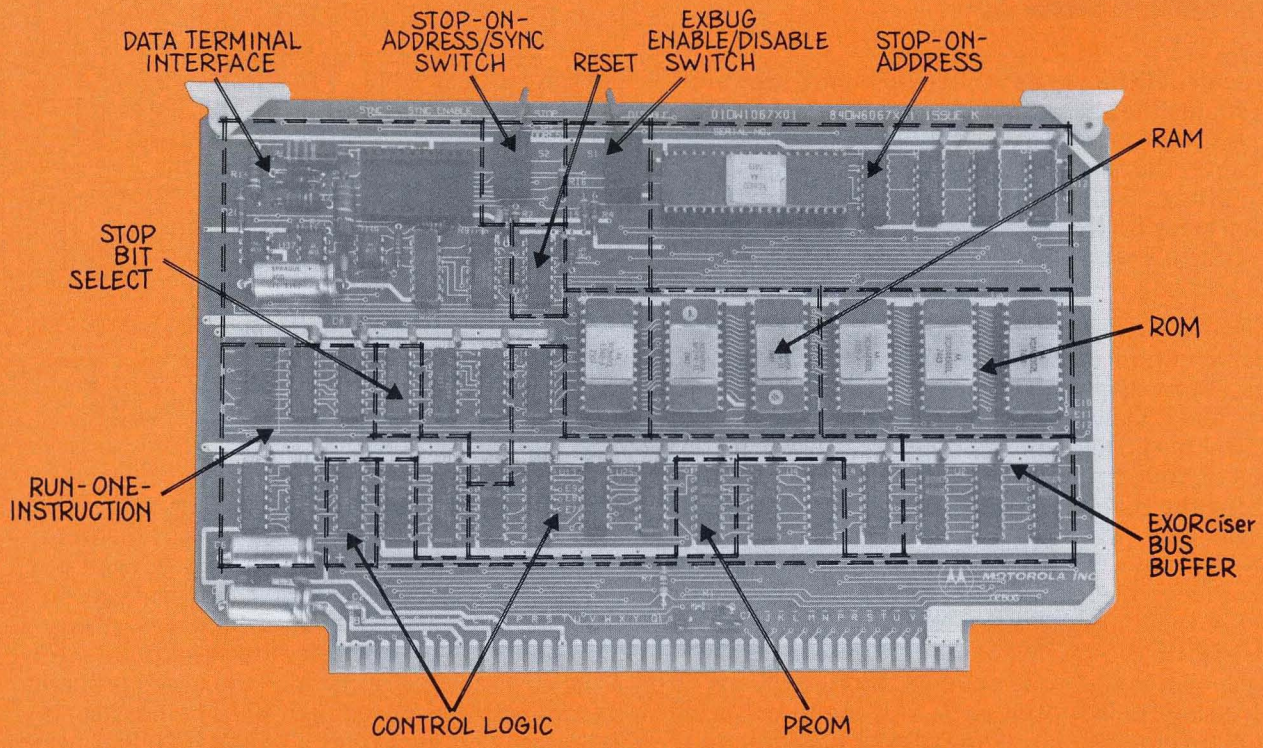
Specifications

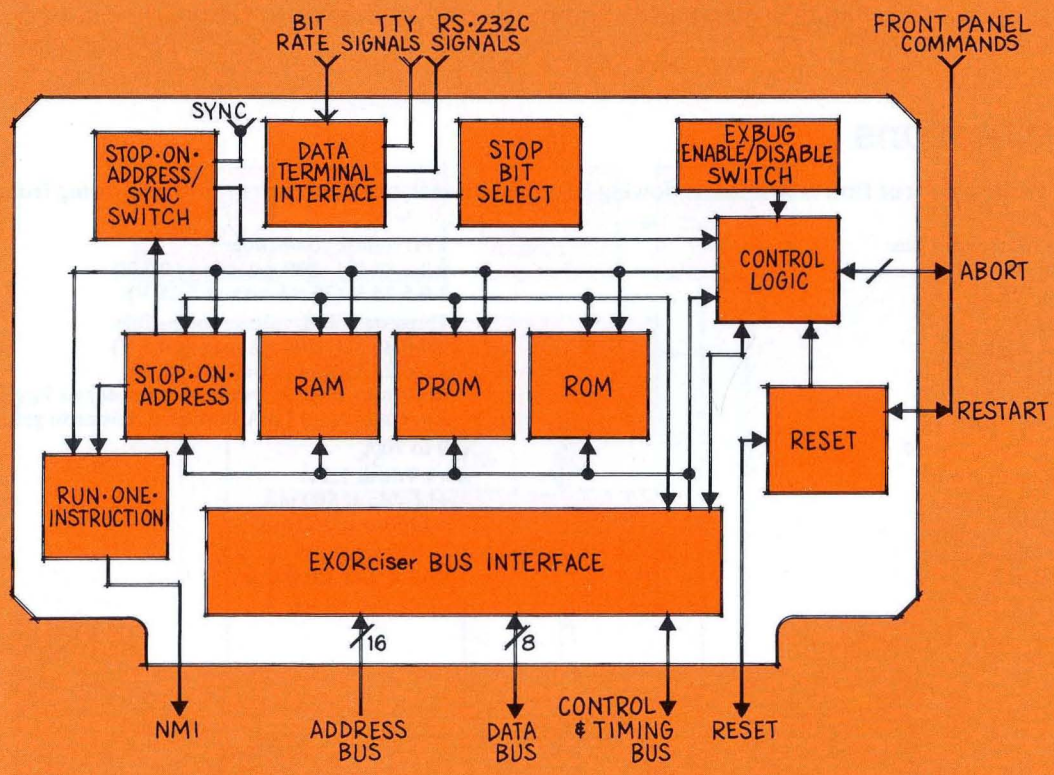
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Address and Control Bus	**TTL voltage compatible**
Logic "0"	**0.0-0.85 V (−200 μA max at 0.5 V)**
Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	**0.0-0.85 V (−200 μA max at 0.5 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at −10 mA through a resistor to ground**
Operating Temperature	**0 to 70°C**
Power Requirements	**+5 Vdc at 1.3 A**
	+12 Vdc at 500 mA
	−12 Vdc at 500 mA
Physical Dimensions	
W x H x T	**9.75 x 5.75 x 0.062 in.**

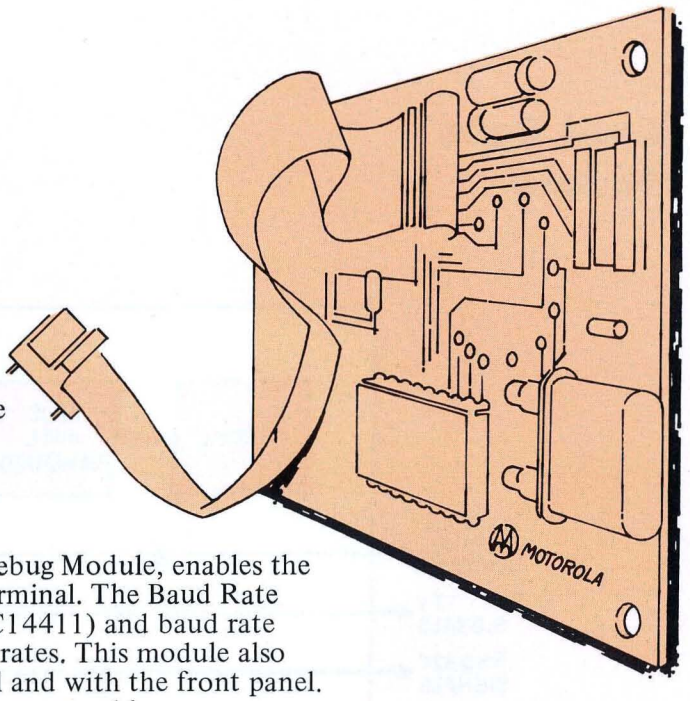
Debug Module

Resident





Baud Rate Module



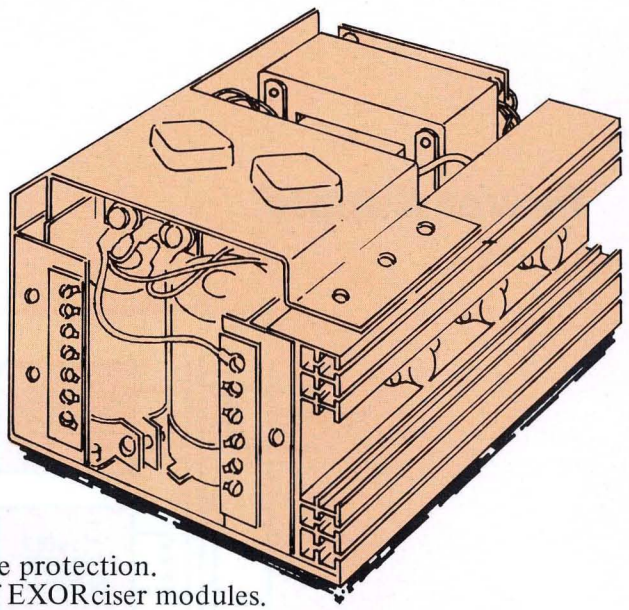
- Provides the EXORciser with eight switch-selectable baud rates between 110 and 9600.
- Provides an interface between the Debug Module and the selected data terminal
- Provides an interface between the front panel and the Debug Module

The Baud Rate Module, in conjunction with the Debug Module, enables the designer to communicate with EXbug via a data terminal. The Baud Rate Module's crystal oscillator baud rate generator (MC14411) and baud rate switch provide the EXORciser with eight standard rates. This module also interconnects the Debug Module to a data terminal and with the front panel. Included with the module is the front panel interconnect cable.

Specifications

Baud Rates: (Switch Selectable)	**110,150,300,600,1200, 2400,4800, and 9600**
Physical Dimensions: W x H x T	**3.688 x 5.25 x 0.062 in.**

Power Supply



- Provides all required EXORciser voltages
- Capable of supporting a full EXORciser rack of Modules

The power supply provides the EXORciser with +5 Vdc, +12 Vdc and -12 Vdc power sources. The +5 Vdc regulated source has both overload and overvoltage protection. This power source is capable of driving a complete rack of EXORciser modules.

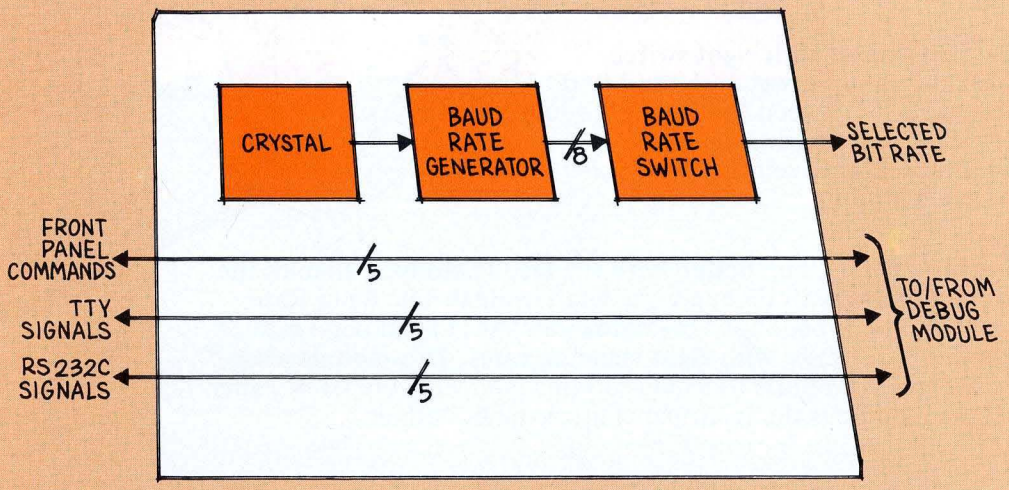
The +12 Vdc and -12 Vdc sources are used to power portions of the interface circuitry between the EXORciser and a data terminal. These sources have overload protection and may be used to power custom circuitry on other modules.

Specifications

Output Voltages:	**+5 Vdc @ 15 A**
	-12 Vdc @ 1.5 A
	+12 Vdc @ 2.5 A
Input Voltage:	**95-125/205-250 Vac**
Input Frequency:	**47 to 420 Hz, Single Phase**
Physical Dimensions: L x W x H	**9.50 x 6.25 x 5.00 in.**

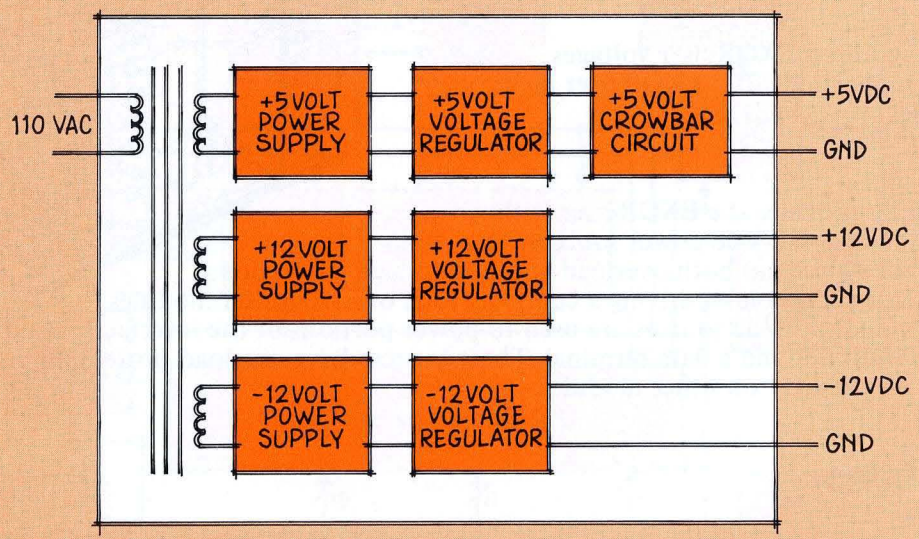
Baud Rate Module

Resident



Power Supply

Resident



MOTOROLA Semiconductor Products Inc.

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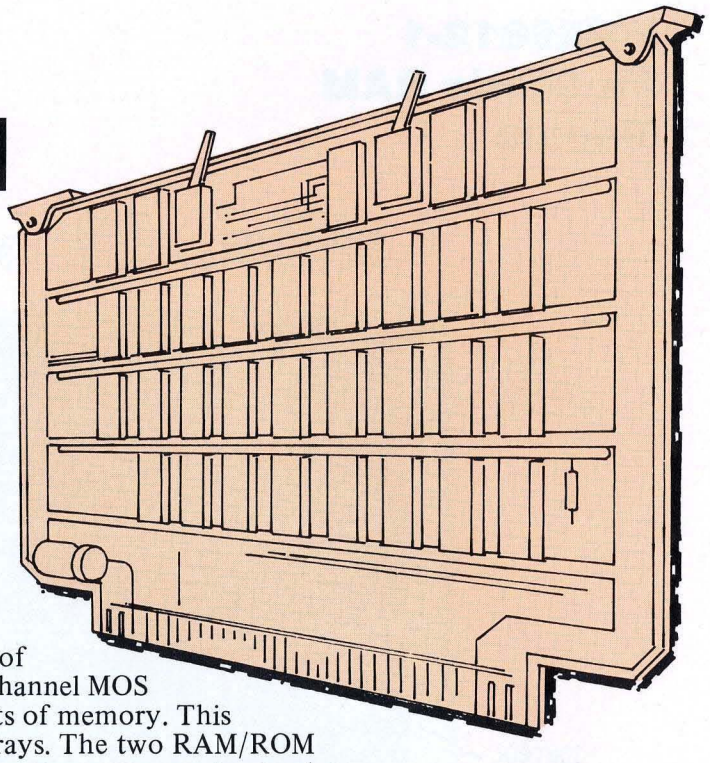
10211 PRINTED IN USA 7-76 IMPERIAL LITHO 858203 20M

MOTOROLA MICROSYSTEMS

MEX6812-1 2K Static RAM Module



- 2048 x 8 bits of static N-channel MOS memory in 1K byte arrays
- Switch-selectable base memory address for each 1K RAM array
- Switch-selectable RAM/ROM (inhibited memory write function) capability for each array
- 500 nanosecond memory access time
- TTL voltage compatible
- Bus interface driver capability

The MEX6812-1 2K Static RAM Module, consisting of sixteen 2102-1 1024 x 1-bit RAMs or equivalent N-channel MOS memories, provides the EXORciser with 2048 x 8 bits of memory. This memory is organized into two separate 1024 byte arrays. The two RAM/ROM switches on the module determine whether their respective arrays are to simulate one (1024 x 8-bit) MCM6830 ROM or eight (128 x 8-bit) MCM6810 RAMs. Three-state bus buffers interface this module to the M6800 MPU over the EXORciser system bus.

The designer can select the base memory address, in 1024 bit increments, for each memory array by setting of the base memory address switches. Address decoders on this module monitor the 16 address lines and determine when the EXORciser's MPU is addressing their respective memory arrays. A logic circuit decodes three inputs, reads the RAM/ROM switches, and determines the memory function to be performed – read data from the memory, write data into the memory, or inhibit the memory write function.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Type Memory	MOS Static RAM
Memory Organization	2048 x 8 bits organized into two 1024 x 8 bit arrays
Memory Cycle Time	500 ns
Input Signals	TTL voltage compatible
Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Power Requirements	5 Vdc @ 1 A Max.
Physical Dimensions W x H x T	9.75 x 5.75 x 0.062 in.

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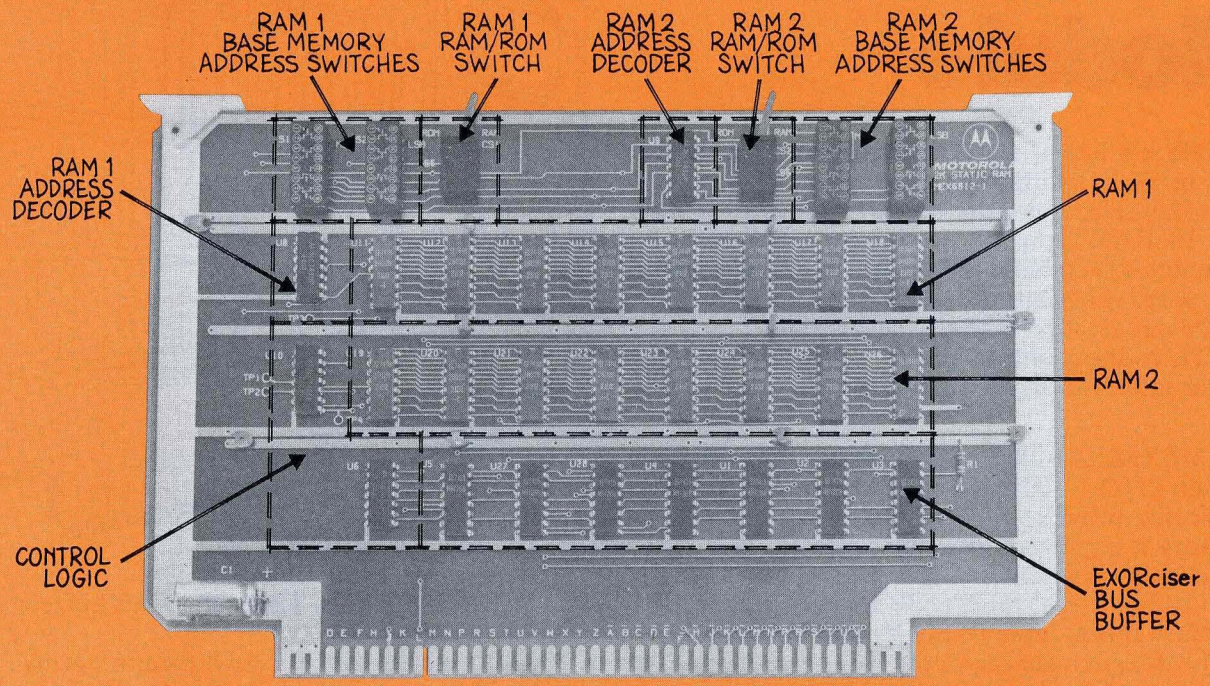
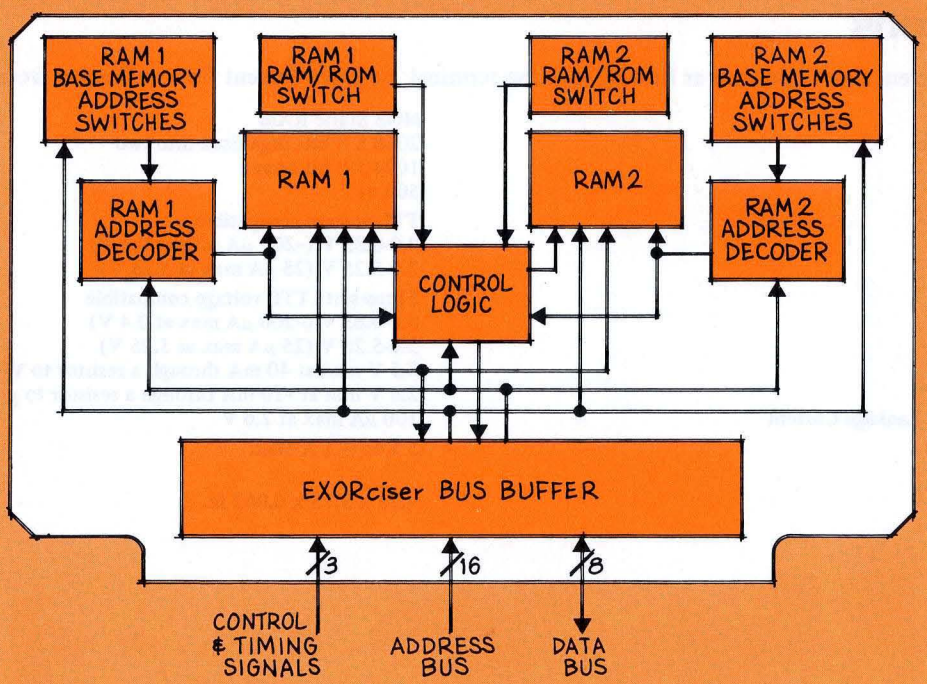
ISSUE A

MEX6812-1
2K Static RAM
Module

Option





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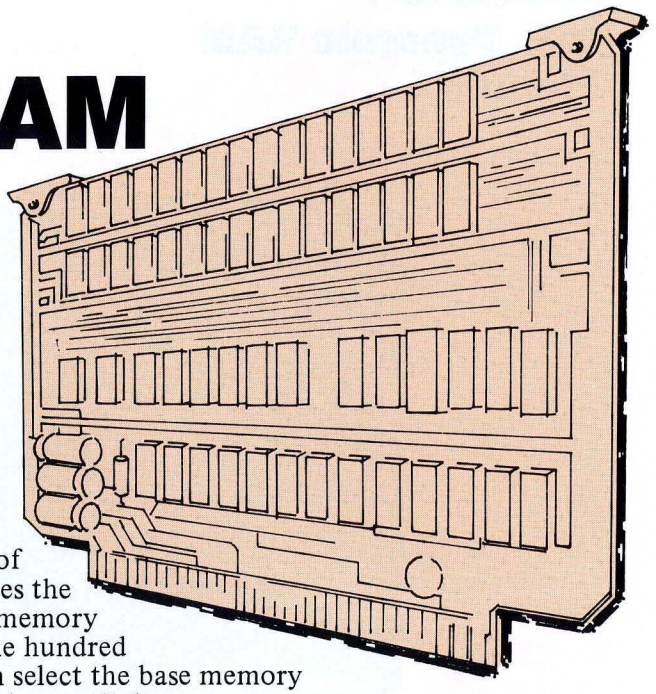
10211 PRINTED IN USA 7-76 IMPERIAL LITHO 858203 20M

MOTOROLA

MEX6816-1 16K Dynamic RAM Module



- 16,384 x 8 bits of dynamic NMOS memory in one array
- Switch selectable base memory address for the memory array
- Cycle stealing memory refresh operation
- Optional even parity capability (consult factory)
- TTL voltage compatible
- Bus drive capability

The MEX6816-1 16K Dynamic RAM Module, consisting of 16 MCM6604L2 N-Channel MOS memory devices, provides the EXORciser with 16,384 bytes of dynamic memory. This memory is organized into one 16K memory array and simulates one hundred twenty-eight 128 x 8 bit MCM6810A RAMs. The user can select the base memory address for this array through setting the base memory address switches.

The address multiplexer in a refresh operation selects the memory location to be refreshed. During normal operation this circuit transfers its six address inputs to the EXORciser bus buffer. The EXORciser bus buffer latches its address input. The address decoder determines when the MPU is addressing its memory array and enables the control logic circuits. The control logic now decodes its control and timing inputs and determines the module's operation. Working with the EXORciser bus buffer, it controls the address multiplexing required by the MCM6604L2 devices. The control logic also decodes the Read/Write command and determines whether the module is to perform a memory read or memory write operation.

The control logic initiates a memory refresh operation once every 32 μs and the module refreshes its memory on a cycle stealing basis.

The optional parity circuit generates a parity bit during a memory write operation and checks that data during a memory read operation. On detecting a parity error, the circuit generates the PARITY ERROR and $\overline{\text{PARITY ERROR}}$ flag signals. Consult the factory for details on this option.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Type	N-channel MOS dynamic RAM (MCM6604L2 devices)
Memory Organization	8,192 x 8 bits, 12,888 x 8 bits, or 16,384 x 8 bits organized into one array
Parity	Optional even parity – consult factory
Read Access Time	350 ns from row address strobe (approximately 300 ns from memory clock)
Input Signals	TTL voltage compatible
Control Lines	
Logic "0"	0.0-0.85 V (-200 μA max at 0.4V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Address	
Logic "0"	0.0-0.8 V (-2.0 mA max at 0.5 V)
Logic "1"	2.0-5.25 V (1.0 mA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at -40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Operating Temperature	0 to 70° C
Power Requirements	+5 Vdc at 1.5 A max +12 Vdc at 1.6 A max -12 Vdc at 110 mA max
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

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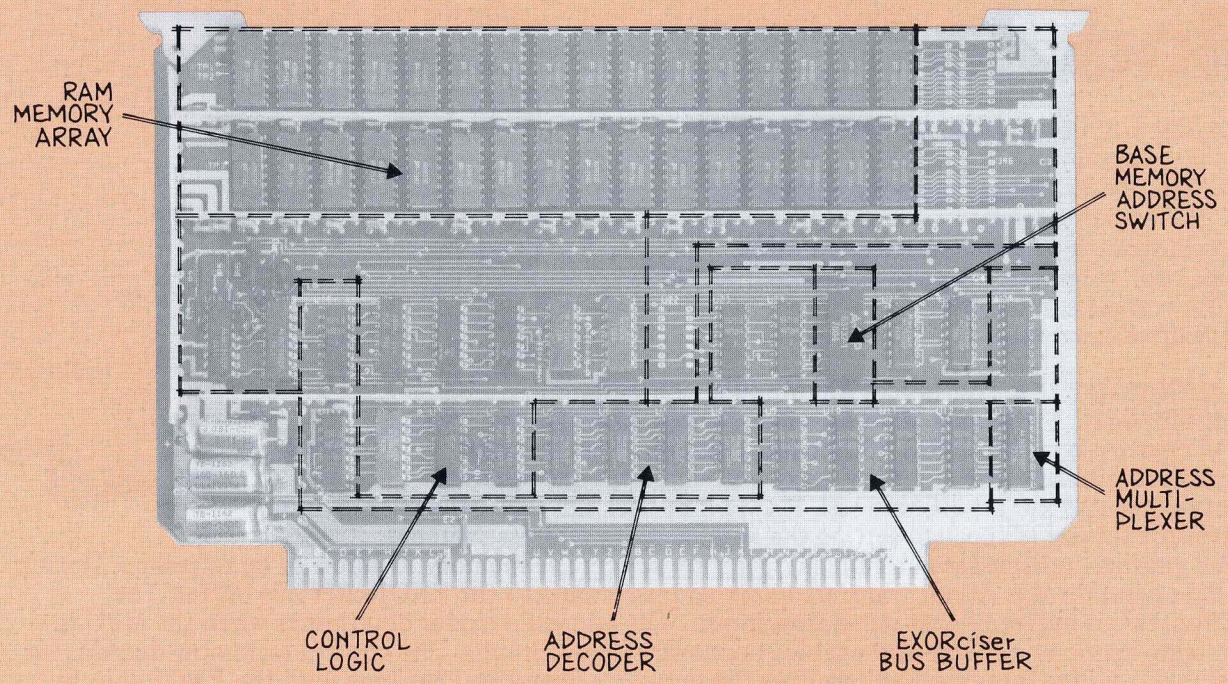
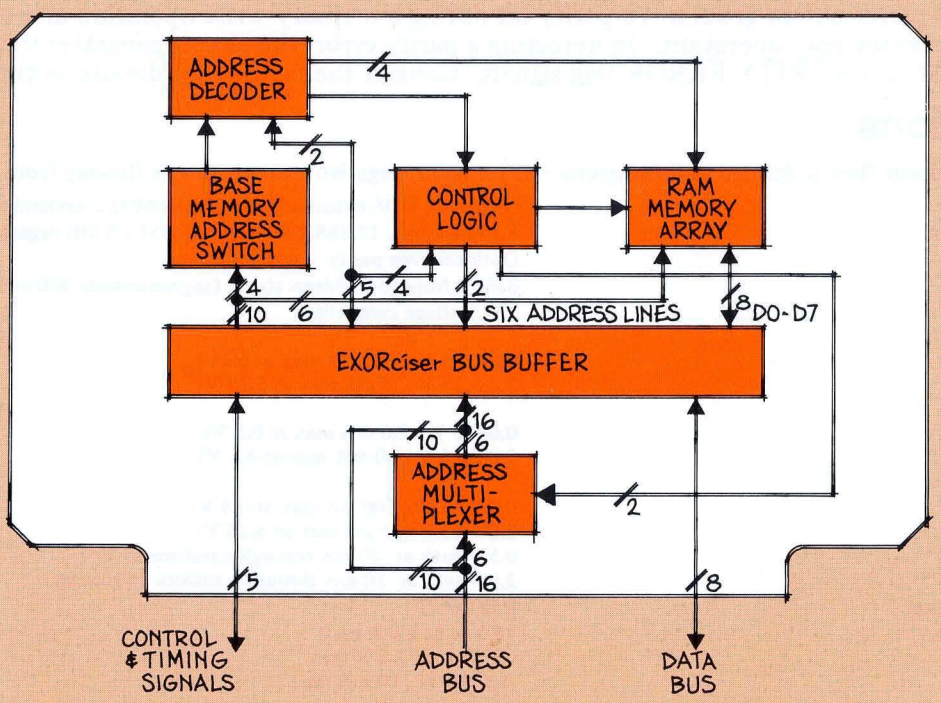
ISSUE A

MEX6816-1
16K Dynamic RAM Module

Option





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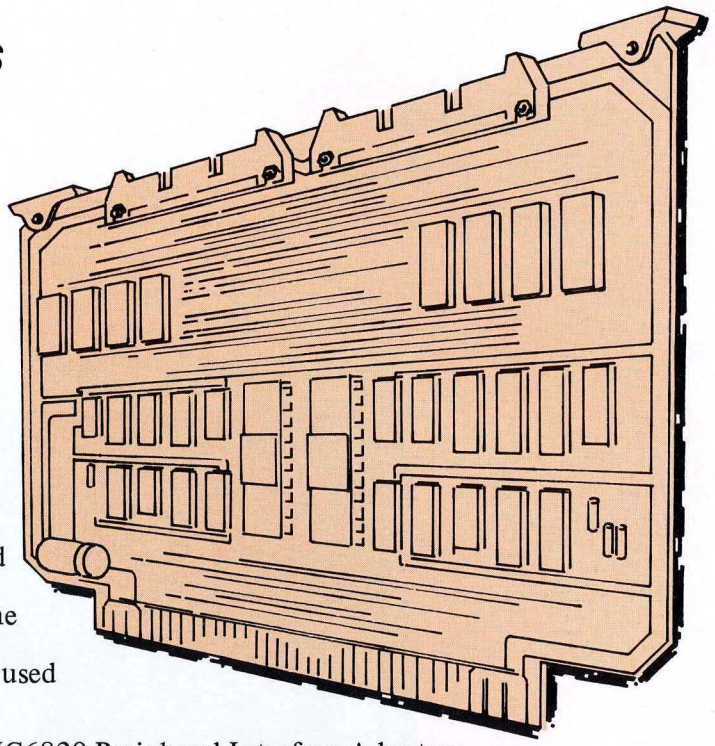
MOTOROLA MICROSYSTEMS

MEX6820 Input/Output Module



- Four 8-bit input/output ports for peripheral interfacing
- Eight individually controlled interrupt lines – four of which may be used as peripheral control lines
- Program controlled maskable interrupt capability
- Each MC6820 Peripheral Interface Adapter addressed as memory
- Switch selectable base memory address for each of the two MC6820 Peripheral Interface Adapter devices
- Provisions on the module for wirewrap sockets to be used in constructing custom interface circuitry

The MEX6820 Input/Output Module, containing two MC6820 Peripheral Interface Adapters (PIA's), provides a flexible means of interfacing the EXORciser with a user's defined process or peripheral device. This module, in effect, connects the two PIA's between the MPU and the peripheral device(s). The designer has the option of interfacing a peripheral directly to the PIA's TTL voltage compatible I/O ports and control lines, or through custom interface circuitry. (The peripheral interface lines of the PIA are PA0-PA7, PB0-PB7, CA1, CA2, CB1, and CB2.) The I/O Module has provisions for standard 14, 16, and 24 pin wirewrap sockets, thus permitting the construction of custom interfacing circuits on the module.

The EXORciser's MC6800 MPU addresses each of the PIA's as four locations in memory. Address switches allow the user to select base memory locations for each PIA. Altering the settings of the address enable/disable switches sets up the Input/Output Module to emulate a design that may or may not use all 16 address lines. Address decoders determine when the MPU is addressing a particular PIA's register and also signal the control logic to decode its inputs. The control logic, by decoding the MPU timing and control signals, manages the data flow through the I/O Module's buffers. These three-state buffers interface the I/O Module to the MC6800 MPU over the EXORciser bus.

MEX68IC I/O Interconnection Cables are used to connect an Input/Output Module to a peripheral. One end of this flatribbon cable is terminated with a 50-pin flatribbon connector; the other end is not terminated. Two MEX68IC cables should be ordered with each MEX6820 Input/Output Module.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Input Signals	**TTL voltage compatible**
Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at -10 mA through a resistor to ground**
Output Off-State Leakage Current	**100 μA max at 2.6 V**
MC6820 Peripheral Interface Adapter Signals*	
PA0-PA7 Input/Output Lines	**TTL voltage compatible**
PB0-PB7 Input/Output Lines	**Three-state TTL voltage compatible**
CA1, CA2, and CB1 Control Signals	**TTL voltage compatible**
CB2 Control Signal	**Three-state TTL voltage compatible**
IRQA and IRQB Signals	**TTL voltage compatible**
Operating Temperature	**0 to 70°C**
Power Requirements	**5 Vdc at 2 A max**
Physical Dimensions	
W x H x T	**9.75 x 5.75 x 0.062 in.**

***See MC6820 data sheet for specifications on these signals.**

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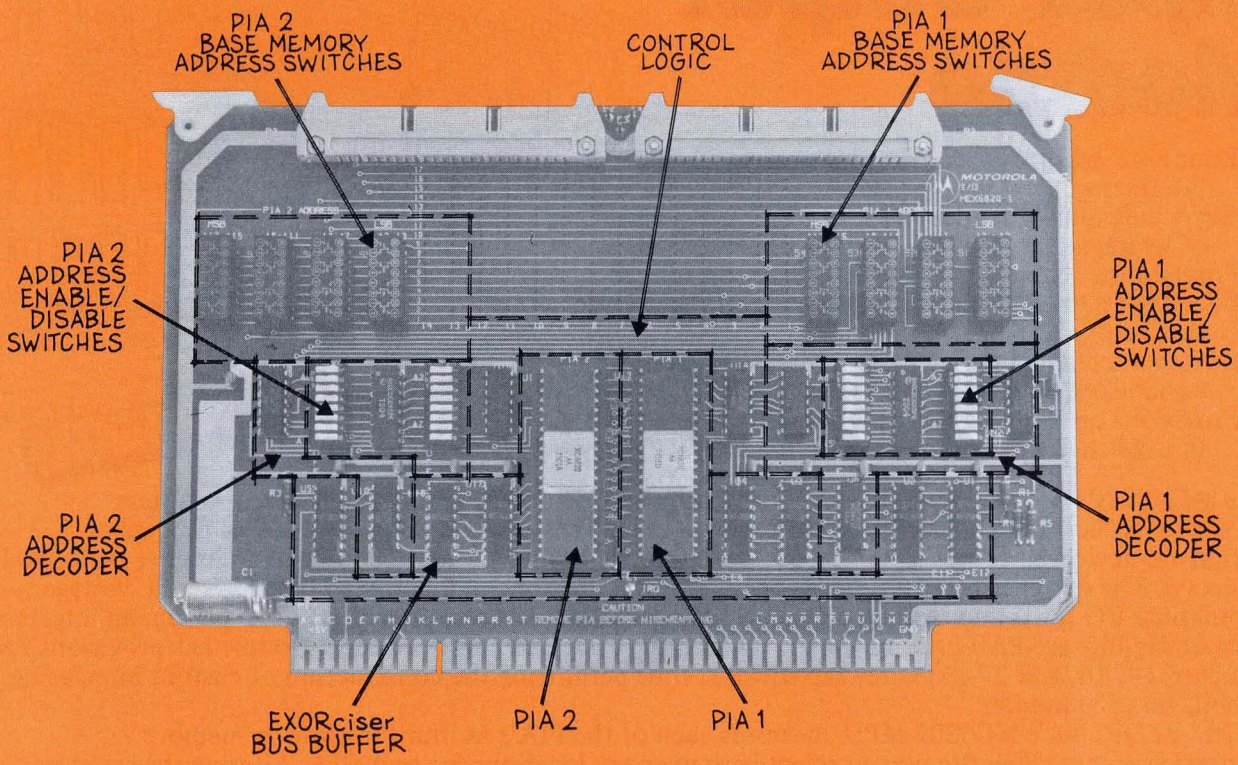
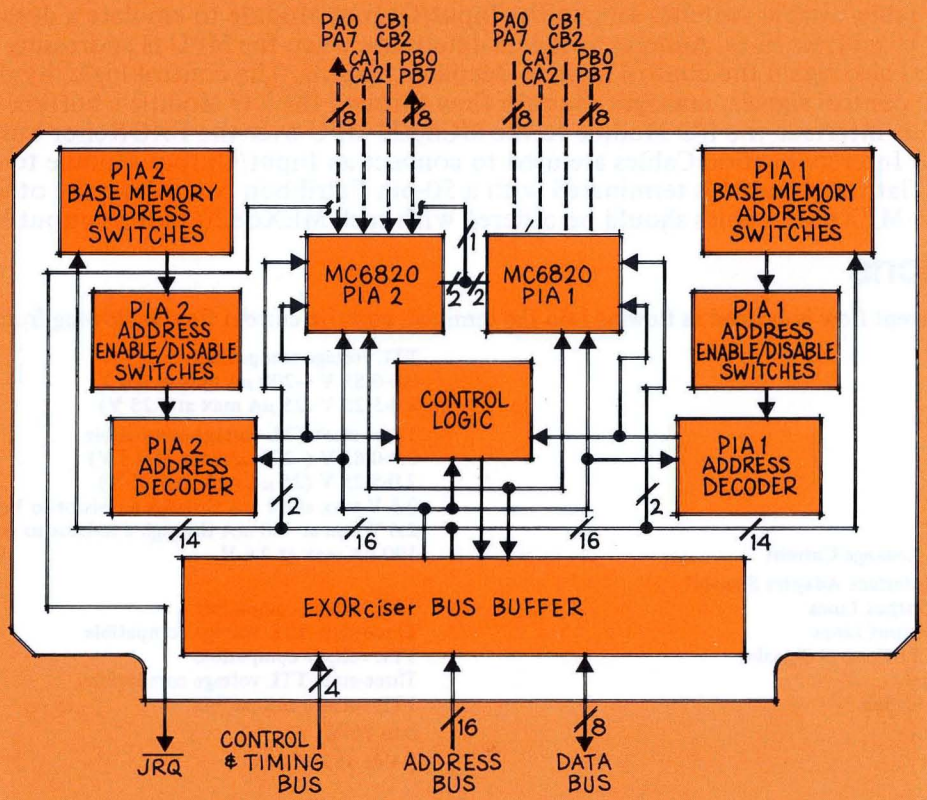
ISSUE A

MEX6820 Input/Output Module

Option





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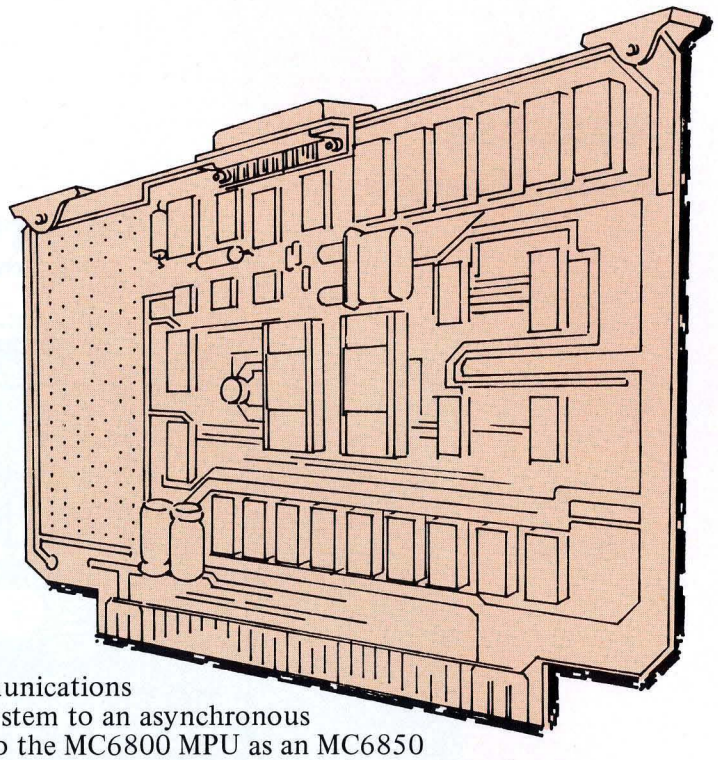
MEX6850 ACIA Module



- Eight or nine-bit transmission
- Program-selectable odd, even, or no parity
- TTY and RS-232C data terminal interface capability
- Program-selectable divide-by 16 and 64 clock modes
- Program-selectable one or two stop bits
- Eight switch-selectable baud rates between 110 and 9600 baud

The MEX6850 ACIA Module (Asynchronous Communications Interface Adapter) interfaces the EXORciser base system to an asynchronous data communications device. This module appears to the MC6800 MPU as an MC6850 ACIA. In preparing a program for this module, the designer determines parity, the number of stop bits and the ACIA's clock mode. The user can select one or two stop bits; odd, even, or no parity; the clock mode; and the number of data bits to be transferred.

The user, in setting up this module, selects one of the eight standard switch selectable baud rates between 110 and 9600. He has the option of interfacing directly with a TTY (20 mA neutral current loop), and an RS-232C compatible terminal, or of constructing a custom interface circuit for some other peripheral. The module can be configured to appear as a data terminal or modem to an external communications device. It has provisions for standard 14, 16, and 24 pin wirewrap sockets to allow for the construction of customized circuits.

The EXORciser's MPU addresses the ACIA as if it were two locations in memory. By proper setting of the base memory address switches, the user can select the base memory address for the ACIA. The address enable/disable switches activate or de-activate individual address lines. This allows the EXORciser to emulate systems not using all 16 address lines. The address decoder determines when the MPU is addressing its ACIA and enables the control logic to decode its inputs. The control logic, by decoding of the MPU timing and control signals, controls the flow of data through the EXORciser bus buffer. The EXORciser bus buffer interfaces the ACIA Module with the EXORciser bus.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Address and Control Bus	**TTL voltage compatible**
Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Data Bus	**Three-state TTL voltage compatible**
Input Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at -10 mA through a resistor to ground**
Output Off-State Leakage Current	**100 μA max at 2.6 V**
Switch selectable baud rates	**110, 150, 300, 600, 1200, 2400, 4800, and 9600**
Signal Characteristics	**TTY (20 mA neutral current loop) or EIA RS-232C compatible**
TTY Reader Control Signal	**Control signal for TTY devices modified for external control**
RS-232 Interface Signals	**RS-232C signals to interface with an RS-232C data terminal. Can be modified to interface with any RS-232C modem.**
Power Requirements	**+5 Vdc @ 750 μA +12 Vdc @ 500 μA -12 Vdc @ 500 μA**
Physical Dimensions	
W x H x T	**9.75 x 5.75 x 0.062 in.**

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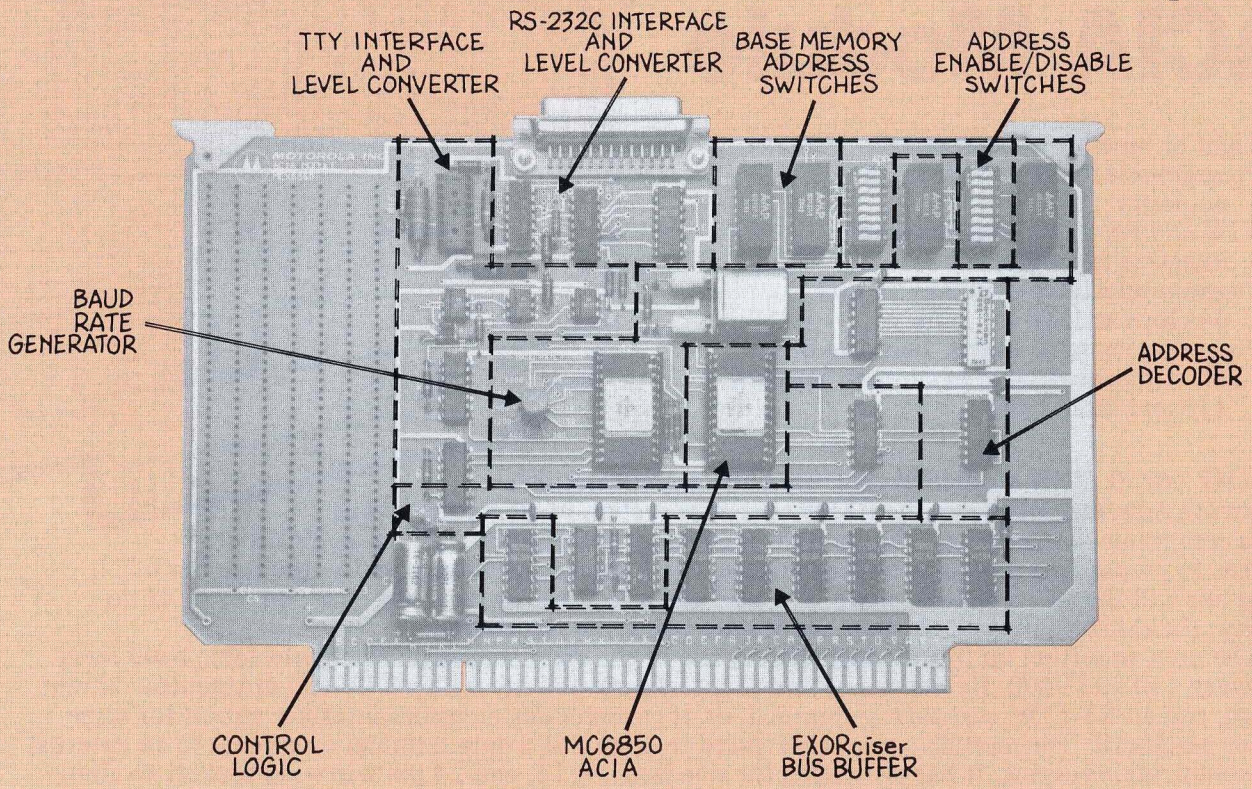
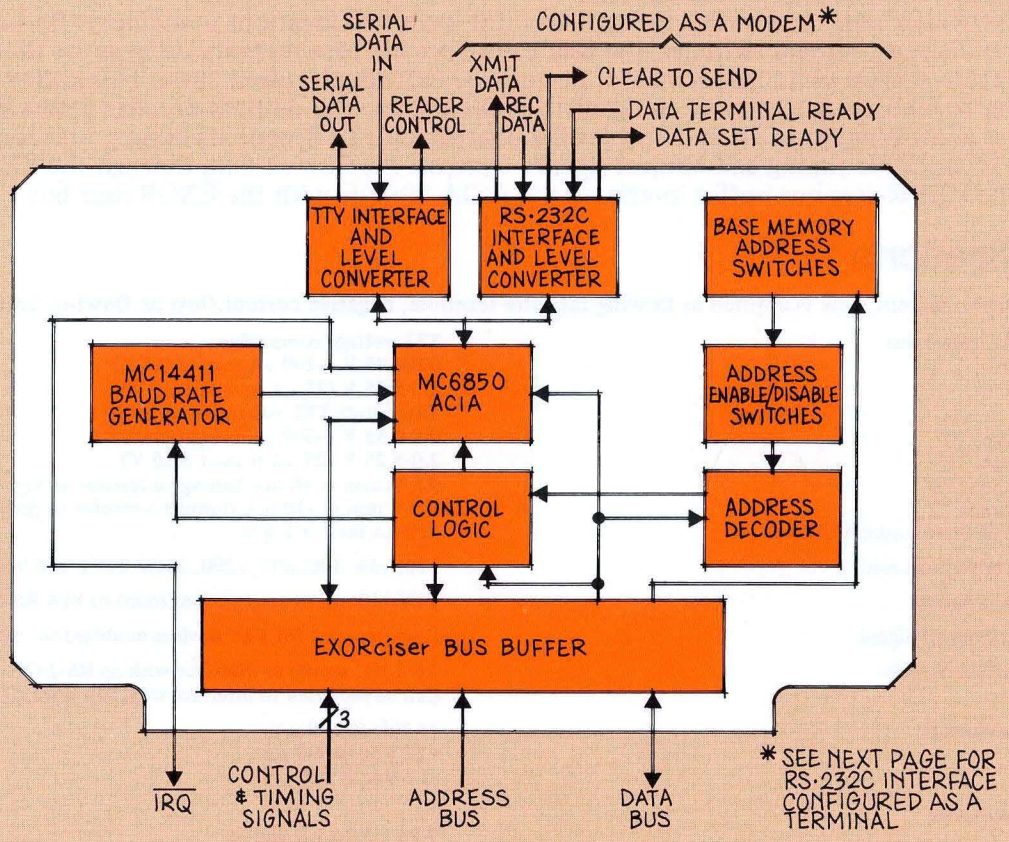
ISSUE A

MEX6850
ACIA Module

Option





Terminal Interface Lines

The user has the option of interfacing the MEX6850 ACIA Module with a TTY (20 mA neutral current loop), an RS-232C compatible terminal, or of constructing a custom interface circuit. In interfacing an RS-232C communications device with the module, the user also has the option of configuring the module to appear as a terminal or as a modem.

TTY Interface Signals

Serial Data In – This line accepts the input from a TTY terminal.

Serial Data Out – This line transfers data to a TTY terminal.

Serial Data Common – This line provides a return for the Serial Data In and Serial Data Out signals.

Reader Control – This signal provides the control required to operate the paper tape reader on a modified manual TTY data terminal.

Reader Common – This line is connected to EXORciser ground and provides a return for the Reader Control signal.

RS-232C Interface Signals

Transmit Data – This line transfers data from a terminal to a modem.

Receive Data – This line transfers data from a modem to a terminal.

Clear to Send – This signal, when high, indicates that the modem is ready to transmit data.

Request to Send – This signal prepares the modem for data transfer. When high, this signal places the modem in the transmit mode; when low, in the receive mode.

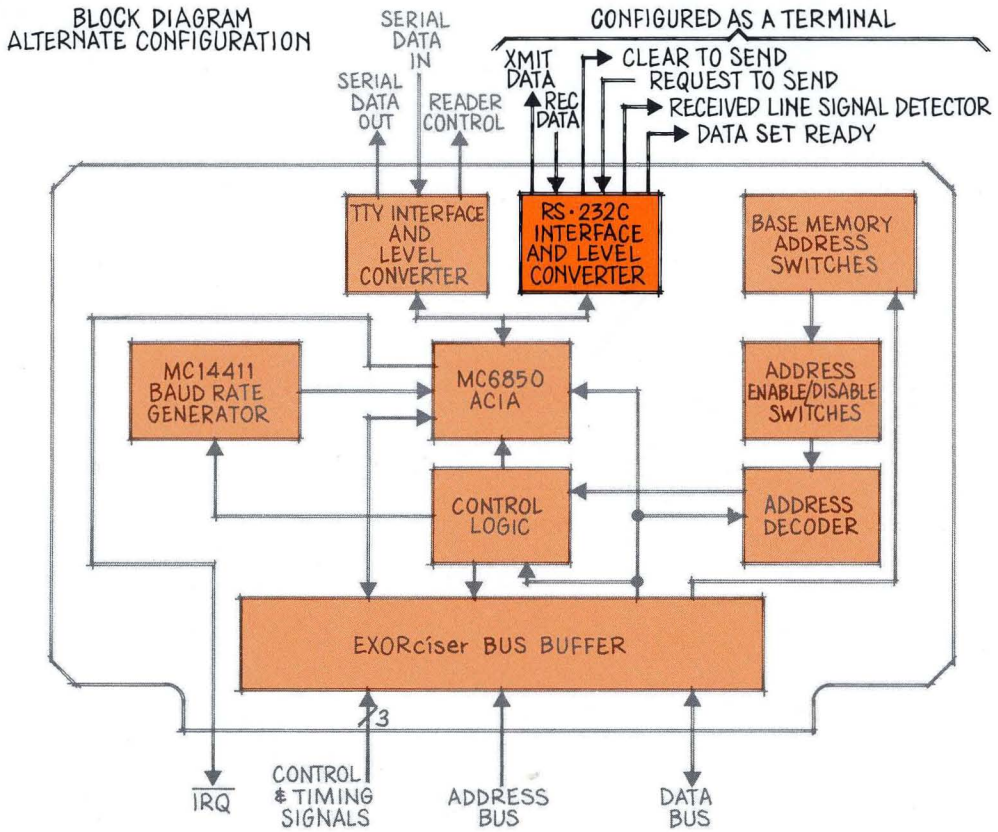
Data Terminal Ready – This line, when high, indicates to the modem that the terminal connected into the system is ready to receive or transmit data.

Data Set Ready – This signal is a high level when the modem is connected to the terminal and indicates to the terminal that the modem is ready.

Received Line Signal Detector – This signal, also called carrier detect, is a high level when the modem is receiving a signal meeting its criteria.

Power Ground – Common for the 12 volt source. This line provides a safety ground connection between the RS-232C compatible communications device and the EXORciser.

Signal Ground – This line provides a common signal connection to the RS-232C communications device.



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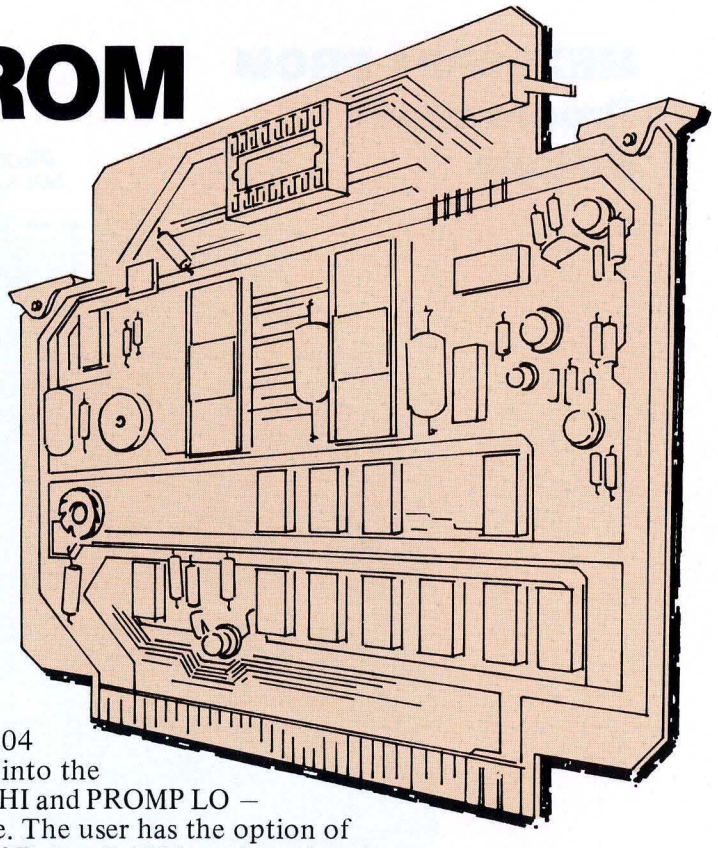
MOTOROLA

MEX68PP1 PROM Programmer Module



- Mounts directly into the M6800 EXORciser
- Program compatible with the EXORciser's EXbug Firmware
- Programs 2704 and 2708 EPROM devices
- EPROM program verification and compare capability
- Capable of moving data from the EPROM to EXORciser memory
- Capable of moving a block of data from one memory location to another
- All programming activities entered and controlled by the EXORciser

The MEX68PP1 PROM Programmer Module provides the EXORciser with the capability of programming 2704 and 2708 EPROM devices. This module plugs directly into the M6800 EXORciser bus and its two programs – PROMP HI and PROMP LO – are compatible with the EXORciser's EXbug Firmware. The user has the option of selecting and locating the PROM program into the EXORciser RAM locations that do not conflict (using the same addresses) with the user's program. That is, if the user has his program loaded in the upper portion of memory, he selects and loads the PROMP LO program into the EXORciser.

The PROM Programmer Module with its software enables the EXORciser to program an EPROM device, to verify the data in the EPROM, to transfer data from the EPROM to the EXORciser's RAM memory, and to transfer blocks of data from one memory location to another.

Specifications

Programs EPROM devices	2704 and 2708
Average Programming Time: 2704	0.57 minute
2708	1.54 minutes
Input Control Signals	TTL Voltage Compatible
Logic "0"	0.0 -0.8 V
Logic "1"	2.0-5.25 V
Address Bus and R/W	
Logic "0"	0.0-0.5 V
Logic "1"	2.4-5.25 V
Off-State Leakage Current	-40 μA
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.8 V (-200 μA at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA at 5.25 V)
Output Logic "0"	0.0-0.5 V (40 mA at 0.5 V)
Output Logic "1"	2.6-5.25 V (-10 mA at 2.6 V)
Output Off-State Leakage Current	100 μA at 2.6 V
Power Requirements	+5 Vdc @ 800 mA +12 Vdc @ 300 mA during programming -12 Vdc @ 50 mA
Operating Temperature	0^{o} to 70^{o}C
Physical Dimensions (W x H x T)	9.75 x 7.50 x 0.062 in.

PROM Programmer Module Options

Option	Part No.	Description
1	MEX68PP1A	PROM Programmer Module with its software on cassette
2	MEX68PP1B	PROM Programmer Module with its software on paper tape
3	MEX68PP1D	PROM Programmer Module with its software on diskette

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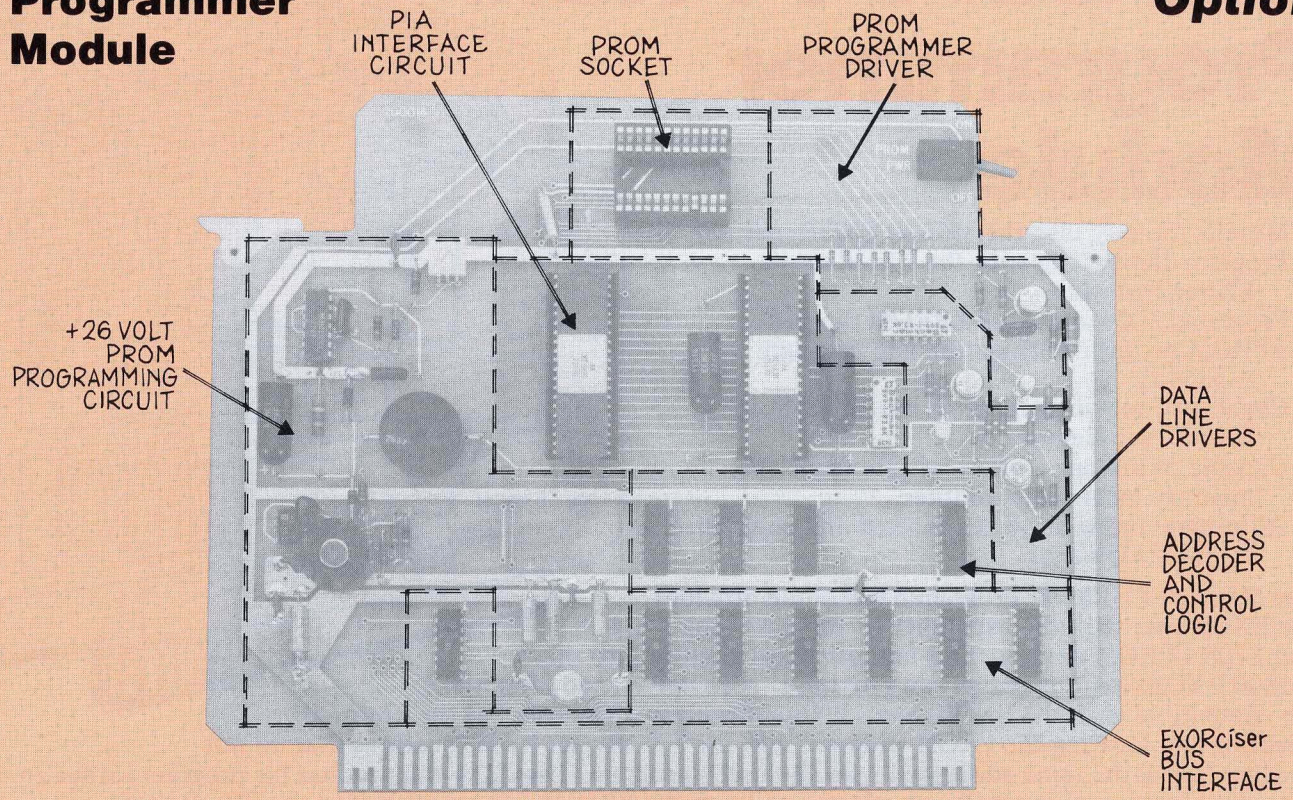
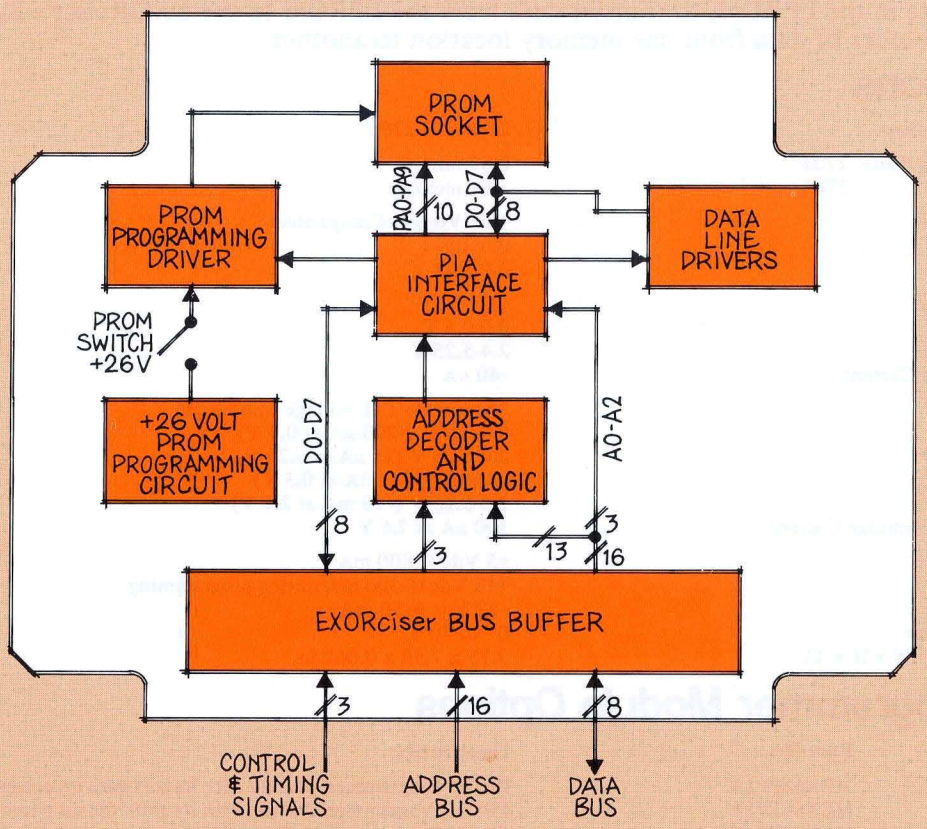
ISSUE A

MEX68PP1 PROM Programmer Module

Option





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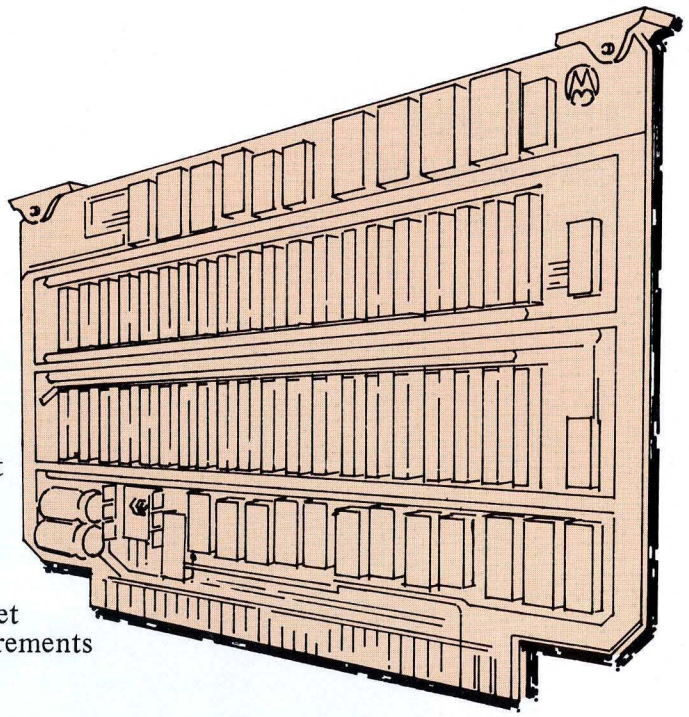
MEX68RR EROM/RAM Module



- Up to 16,384 x 8 bits of ROM/PROM memory in four 4K byte arrays
- Utilizes user-programmed 1024 x 8 bit or 512 x 8 bit ROM/PROM devices (four devices per array)
- Switch selectable base memory address for each memory array
- Switch selectable read enable for each installed ROM and read disable for each unused ROM socket
- Up to 512 x 8 bits of RAM memory in 128 byte increments
- TTL voltage compatible
- Bus drive capability

The MEX68RR EROM/RAM Module provides the EXORciser with up to 16,384 bytes of ROM/PROM memory and up to 512 bytes of RAM memory. Four sockets accommodate up to four MCM6810 128 x 8 bit RAM memory devices. The RAM memory is assigned to memory locations 0000_{16} through $01FF_{16}$ (the bottom of the EXORciser's memory). However, this array consumes the lower 1024 bytes of the EXORciser's memory (0000_{16} through $03FF_{16}$) although the maximum memory capability is 512 bytes.

The ROM memory section is organized into four memory arrays with four sockets per array; therefore each array is capable of mounting up to 4K bytes of ROM or PROM memory. The user installs his programmed ROMS into the desired sockets, and selects the address for each array by proper setting of each array's base memory address switch.

The 16 individual ROM read switches permit the user to enable the ROM/PROM devices to be read and disable the sockets not being used. Unless disabled by this switch, each ROM/PROM socket occupies 1024 bytes of memory whether the device mounted in the socket is a 512 byte or 1024 byte device. The memory locations assigned to the disabled sockets may be assigned to other memory or peripheral devices in the user's system.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Mounting Capability	
RAM	Up to four MCM6810 or equivalent RAM devices (up to 512 bytes)
ROM	Up to 16 MCM68708 or equivalent EROM devices (up to 16K bytes)
Memory Organization	
RAM	Up to 512 x 8 bits organized into one array. (The array consumes 1024 x 8 bits of memory.)
ROM	Up to 16,384 x 8 bits organized into four arrays (four sockets per array), with up to 4096 x 8 bits per array. Unless disabled, each socket consumes 1024 x 8 bits of memory whether it contains a 512 x 8 bit or 1024 x 8 bit ROM/PROM device.
Input Signals	TTL voltage compatible
Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Data Bus	Three-state TTL voltage compatible
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6V
Operating Temperature	0 to 70° C
Power Requirements	+5 Vdc at 1A max +12 Vdc at 1A max -12 Vdc at 1A max
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

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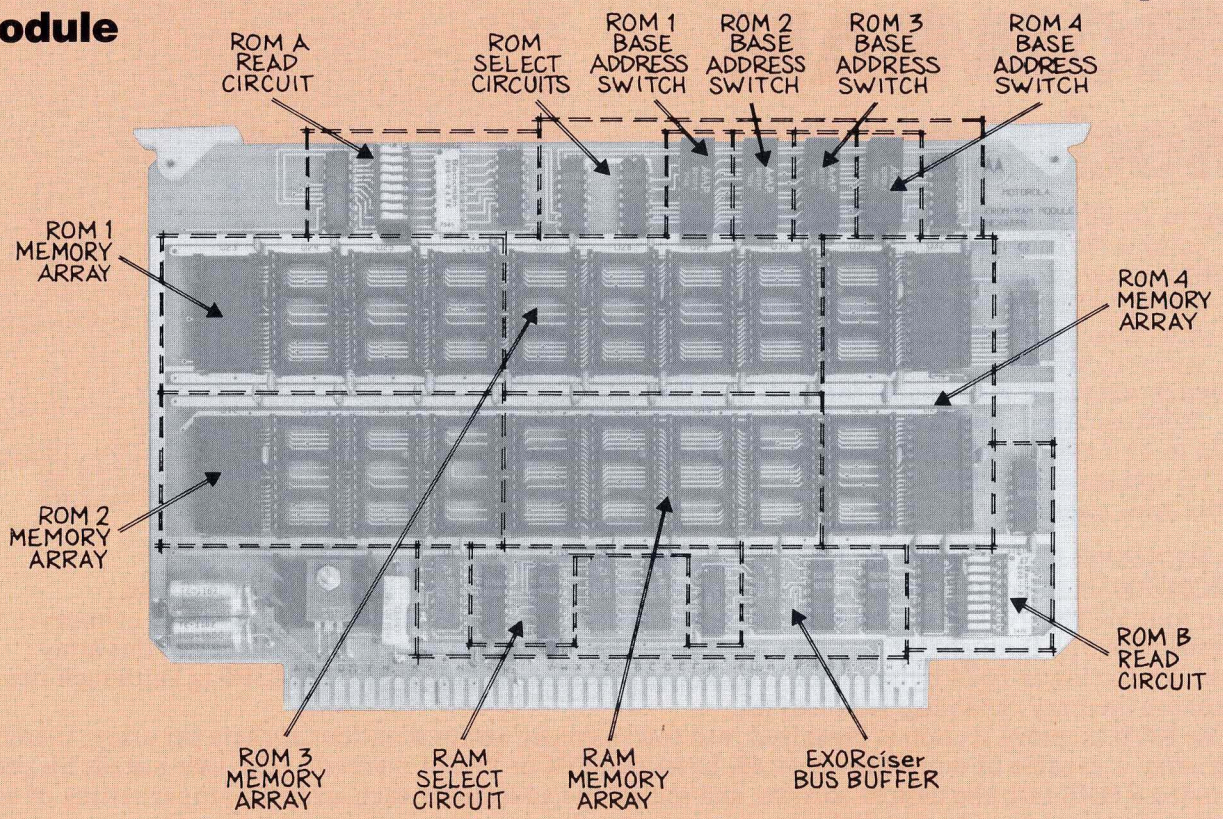
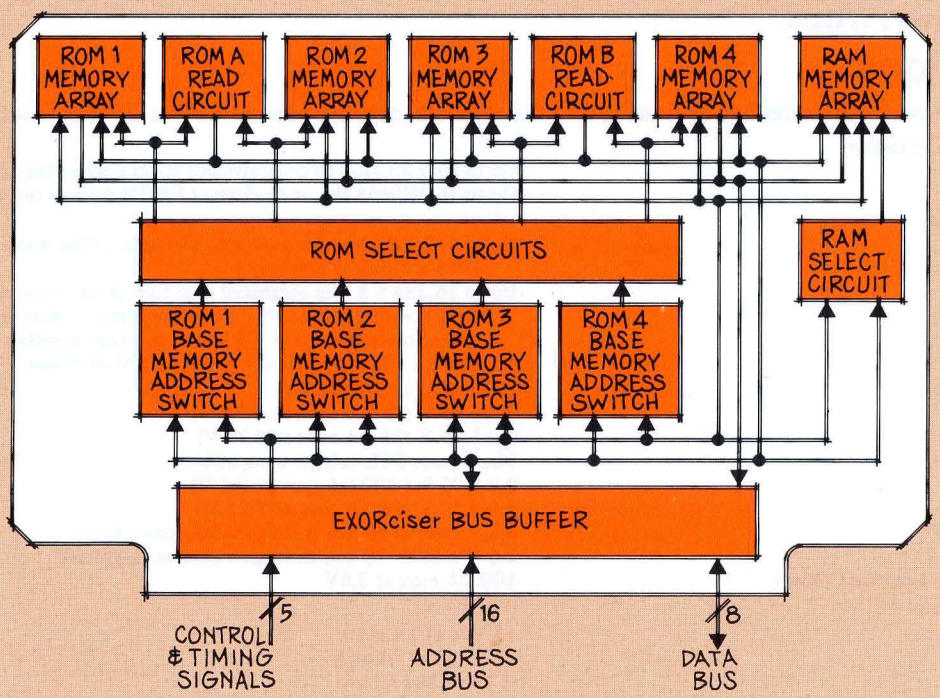
ISSUE A

MEX68RR EROM/RAM Module

Option





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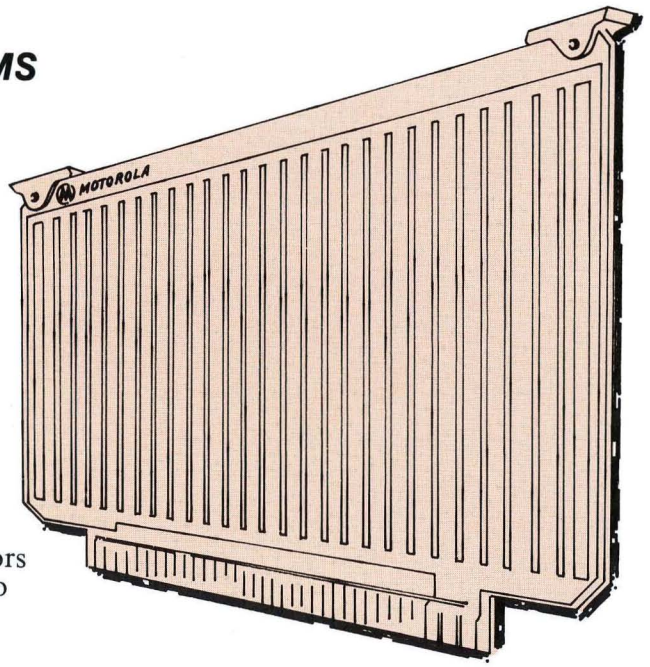
MOTOROLA MICROSYSTEMS

MEX68WW Wirewrap Module

Option



- Standard size EXORciser plug-in module
- Compatible with the EXORciser bus
- Standard pin spacing for 14, 16, and 24-pin wirewrap sockets
- Provisions for two 50-pin flatribbon cable connectors
- Permits user to incorporate his custom circuits into the EXORciser emulated system

The MEX68WW Universal Wirewrap Module permits the user to construct and incorporate his custom circuits into an EXORciser emulated system. Incorporated on the module are the power bus and the ground bus printed wiring runs. Also, the module has standard pin spacing and provisions for 14, 16, and 24-pin wirewrap sockets and for two 50-pin wirewrap flatribbon cable connectors.

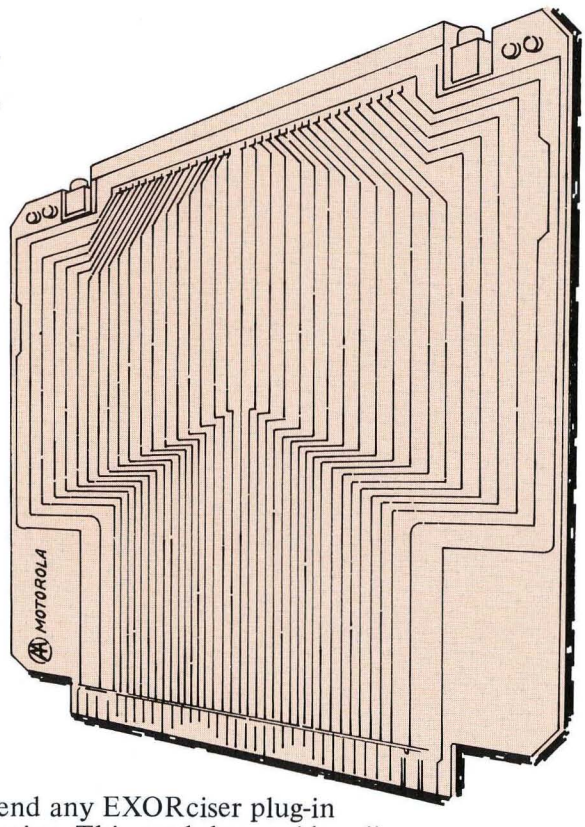
Specifications

Physical Dimensions:

W x H x T	9.75 x 5.75 x 0.062 in.

MEX68XT Extender Module

Option



- Extends any EXORciser plug-in module for testing, trouble-shooting, and debugging
- Interfaces with all EXORciser plug-in modules
- Compatible with the EXORciser bus
- Provides clip-on test points for all EXORciser bus signals

The MEX68XT Extender Module enables the user to extend any EXORciser plug-in module for servicing, testing, trouble-shooting, and debugging. This module provides clip-on test points, giving the user access to the EXORciser bus.

Specifications

Physical Dimensions:

W x H x T	9.75 x 9.00 x 0.062 in.

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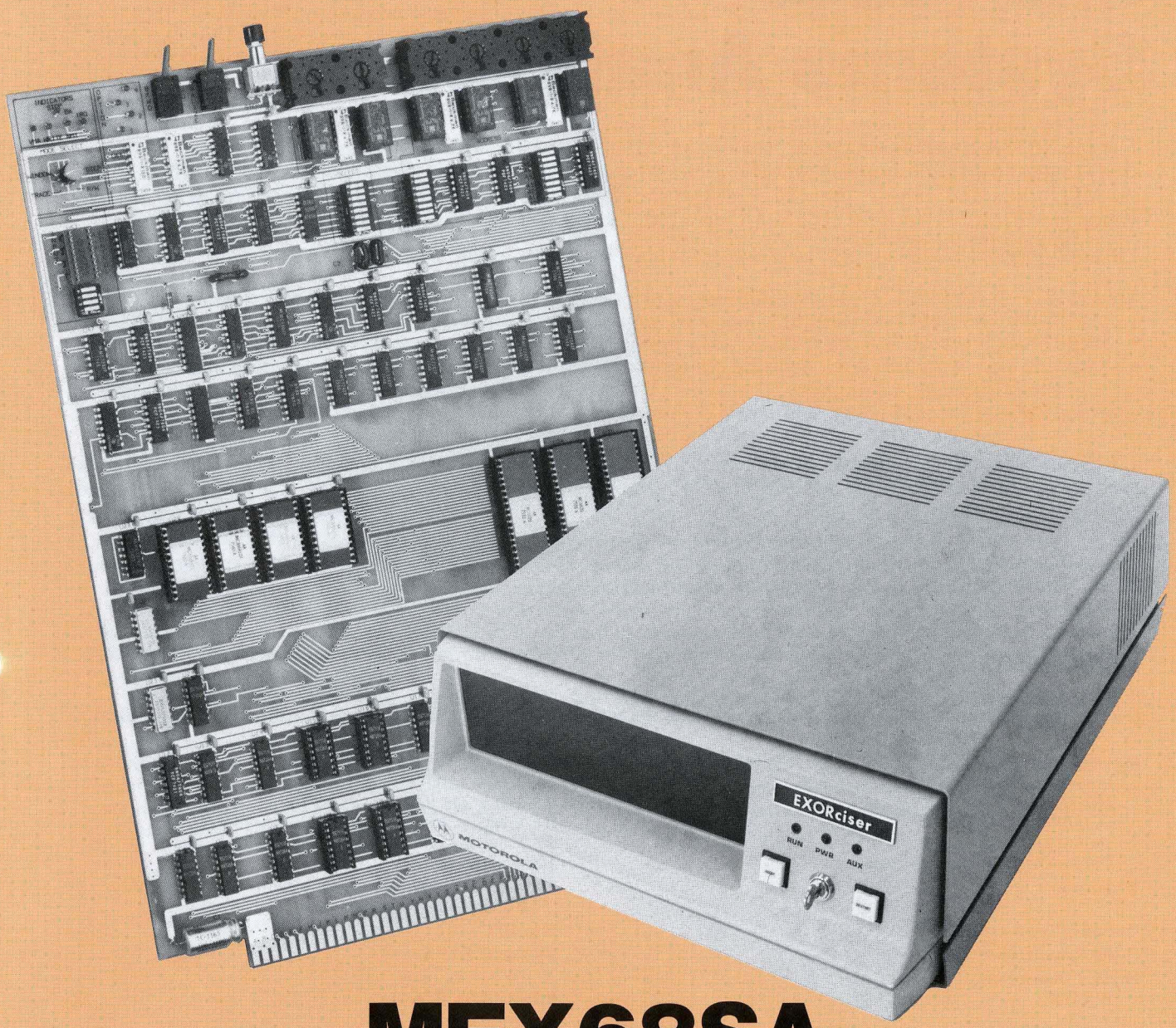
ISSUE A

MOTOROLA



MEX68SA Systems Analyzer

For System Development and Troubleshooting

ISSUE A

MEX68SA Systems Analyzer

The MEX68SA Systems Analyzer provides an efficient and economical means of monitoring, analyzing, and troubleshooting M6800 Microprocessor Systems. This module connects directly into the MPU's bus and permits the user access to the operations being performed inside of his MPU. With a minor modification to the MPU's VMA signal, the Systems Analyzer is capable of performing the following functions:

- Stop the MC6800 MPU on detecting the selected compare conditions
- Step through the MPU's program
- Examine and, if required, change the contents in the MPU system's memory
- Trace through the MPU's program
- Monitor and record (takes a snapshot of) the MPU's operation during a selected portion of the MPU's program
- Print a hard copy of the data stored in the Systems Analyzer memory during the snapshot operation

The Systems Analyzer consists of six major blocks and has six modes of operation. The six major blocks are the Switch and Indicator Section, the Compare Section, the Memory Section, the Bus Buffer Section, the Hard Copy Interface Section, and the Control Section. The Control Section decodes the setting of the MODE SELECT switch and determines the module's mode of operation: MPU Run Mode, Step Mode, Standby Mode, Read/Write Mode, Trace Mode, and Window Mode. The module performs its snapshot operation in the Trace and Window Modes.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Signal Characteristics	
Input Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at -10 mA through a resistor to ground**
Output Off-State Leakage Current	**100 μA max at 2.6 V**
Memory Size	**128 x 32 bits of random access memory consisting of four MCM6810 RAM devices**
Operating Temperature	**0 to 70°C**
Power Requirements	**+5 Vdc @ 2.75 A**
Physical Dimensions	
W x H x T	**9.75 x 14.0 x 0.062 in.**

Systems Analyzer Circuitry

Switch and Indicator Section

This section provides the user with a means of entering the selected compare conditions and of monitoring the status of the MPU bus. The switch portion of this circuitry consists of four hexadecimal address switches, two hexadecimal data switches, and a connector to permit the user to insert up to four optional input signals that he wishes to monitor. The indicator portion of this circuit consists of four hexadecimal address displays, two hexadecimal data displays, and nine LED displays. The LEDs display the status of the MPU (running or halted), the status of the four MPU control signals (R/W, VMA, $\overline{IRQ}$, and $\overline{NMI}$), and the status of the four user-selected optional input signals to the module.

Compare Section

This section, when enabled, compares the MPU bus signals with the output of the hexadecimal switches in the switch and indicator section to detect the selected compare conditions. A switch in each of the compare lines can be enabled or disabled to meet the selected compare conditions. On detecting these conditions, this circuit applies a compare strobe to the other sections in the module.

Memory Section

This section consists of four MCM6810 128 x 8-bit RAM memory devices arranged into a 128 x 32-bit memory array. This memory, when enabled stores the bus status – 16 address lines, 8 data lines, VMA, R/W, $\overline{IRQ}$, $\overline{NMI}$, and the four user selected optional inputs – during each MPU $\phi 2$ clock pulse. The memory is enabled to record data during the snapshot operation in the Trace and Window Modes.

Bus Buffer Section

This section interfaces the Systems Analyzer Module into the EXORciser or the user's system. The data bus buffer devices may be changed to interface the module with a low-true or high-true system.

Hard Copy Interface Section

This section, working with the EXORciser's EXbug Firmware, permits the user to print a hard copy of the data stored in the module's memory. If the Systems Analyzer is not working with the EXORciser, and the user wishes to use the module's hard copy capability, he is required to develop the appropriate I/O routines in his system's program.

Control Section

This section decodes the setting of the MODE SELECT switch and determines which of the module's six modes of operation is to be used.

In the **MPU Run Mode** the Systems Analyzer is disabled and effectively removed from the user's system.

In the **Step Mode** the Systems Analyzer monitors the MPU bus and, on detecting the selected compare conditions, halts the MPU. The user now can step through the user's program.

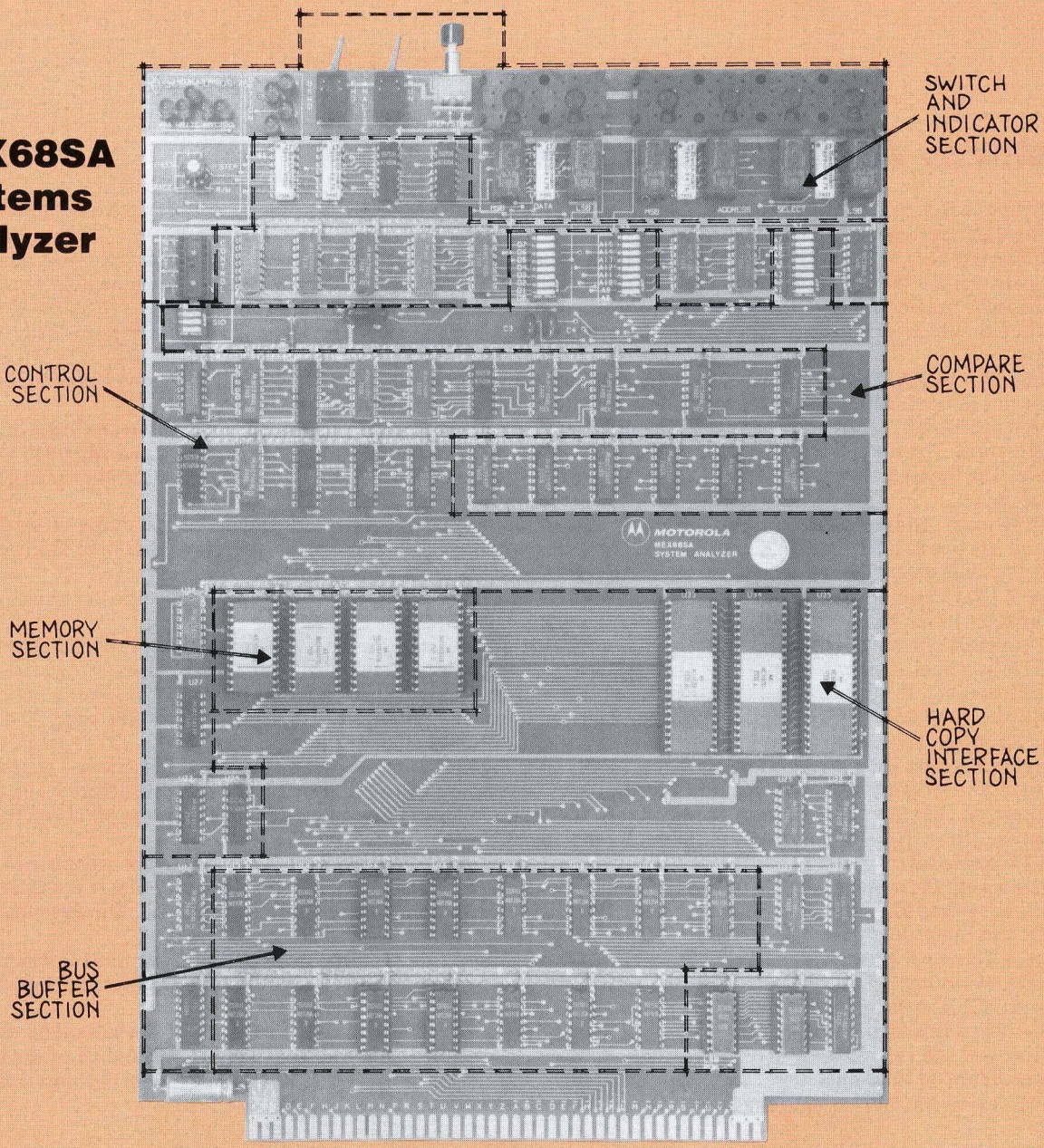
In the **Standby Mode** the Systems Analyzer holds the MPU in the state it was placed in while the module was in the Read/Write or Step Mode.

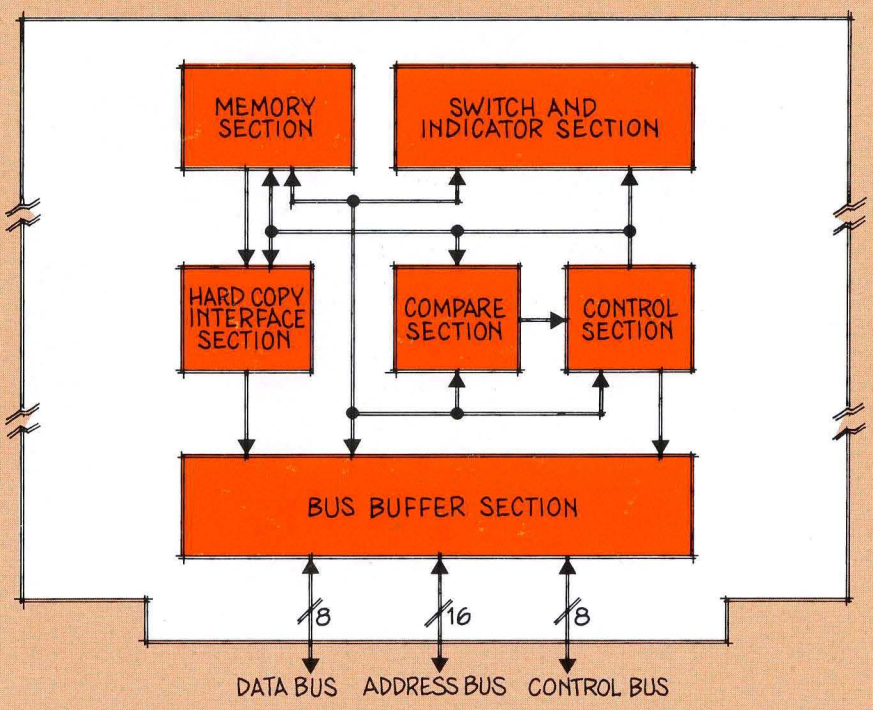
In the **Read/Write Mode** the Systems Analyzer halts the MPU on detecting the selected compare conditions. This module now permits the user to examine and, if required, change the contents in the MPU's memory. The hexadecimal switches in the Switch and Indicator Section select the memory location to be examined and the hexadecimal data switches select the data to be written into memory.

In the **Trace Mode** the Systems Analyzer stores the MPU bus status in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions, the Systems Analyzer stores an additional 64 bus states and then halts the MPU. The user now can examine the 128 bus states – the 63 bus states before the selected compare conditions, the selected compare condition bus state, and 63 bus states after the selected compare conditions – recorded in the module's memory.

In the **Window Mode**, as in the Trace Mode, the Systems Analyzer stores the MPU bus states in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions the module stores an additional 64 bus states and then stops storing data. In this mode, however, the MPU is not halted but continues running and the user has a snapshot or window view of the operations being performed in the selected portion of his program. The user can now examine the 128 bus states within the selected window area and, if desired, print a hard copy of these bus states.

MEX68SA Systems Analyzer





Systems Analyzer Interface Signals

The MEX68SA Systems Analyzer Module plugs directly into the EXORciser bus or may be connected to the MPU's bus in the user's system.

Data Bus (D0-D7) or Data Bus (D0-D7) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module in the EXORciser or the MPU in the user's system and the selected memory location. When the MPU has been halted, the Systems Analyzer controls the flow of data on this bus. These bus signals in the EXORciser are low true. The user can, through installing the appropriate bus device, change these signals for high true operation.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the selected address to the system's memory and input/output devices. When the Systems Analyzer is halted, it controls this line.

Read/Write (R/W) – This MPU output signal indicates whether the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this line is read. Also, when the MPU is halted, this signal will be in the read state. The Systems Analyzer, in halting the MPU, gains control of this signal and can initiate a memory read or write operation.

Valid Memory Address (VMA) – This line, when present, indicates to the memory and peripheral devices that the address on the bus is valid. The MPU's VMA output signal must be modified to allow the Systems Analyzer Module to pull this line high and address the memory and peripheral devices when the MPU is halted.

Phase 2 (ϕ2) Clock Signal – This signal is between 100 kHz and 1 MHz, and is used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU clock.

Bus Available (BA) – This MPU output signal is normally in a low state. When activated, it will go high indicating that the MPU is available. This will occur if the Halt line is low or the MPU is in the WAIT state as the result of executing a WAIT instruction. At such time, all the MPU three-state output drivers will go to their off or high impedance state and all other outputs to their normally inactive state. An interrupt command removes the MPU from the WAIT state. The Systems Analyzer uses this signal to indicate the status of the MPU – halted or running.

Interrupt Request (IRQ) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the system. The MC6800 MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence. The Systems Analyzer monitors this signal.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the system. The MC6800 MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At this time, the MPU will begin its non-maskable interrupt routine. The Systems Analyzer also monitors this signal.

Reset – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when the user resets his systems. This signal, in addition to resetting the system's MPU, is used to reset and initialize the Systems Analyzer's MC6820 Peripheral Interface Adapter devices.

Halt – When this level sensitive signal is low, all activity in the MC6800 MPU will be halted. In the halt mode, the microprocessor will stop at the end of an instruction, the Bus Available signal will be at a high level, and all of the three-state lines will be in their high impedance state. The MPU's VMA signal must be modified to allow the Systems Analyzer Module access to the MPU system's memory and peripherals when it has halted the MPU.

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MOTOROLA MICROSYSTEMS

Advance Information

MEX68USE User System Evaluator (USE)

The MEX68USE User System Evaluator (USE), working with the M6800 EXORciser and the optional MEX68SA Systems Analyzer Module, provides the user with the complete systems development tool. That is, USE extends all of the EXORciser's EXbug functions and all of the optional Systems Analyzer functions into the user's system. The USE-equipped EXORciser provides the designer with the capability of configuring an emulation of his M6800 microprocessor system in the EXORciser, external to the EXORciser, or a combination of EXORciser-mounted modules working with the user's external system. The designer also can develop his system software and firmware on the EXORciser and can use the USE-equipped EXORciser to debug his system hardware and software. In fact, a USE-equipped EXORciser can even be used to test and evaluate the user's production systems.

- Extends the EXORciser EXbug functions into the user's system.
- Operates from the user's system clock or from the EXORciser's internal clock.
- Permits the user to share the EXORciser's memory and input/output modules with the user's system.
- Extends the optional Systems Analyzer Module's functions into the user's system when the Systems Analyzer is used with the EXORciser.
- Provides convenient block/fault isolation.
- Uses present commands – no new protocol to be learned.

USE consists of three assemblies: the USE Processor Module, the USE Intercept Module, and the USE Cable and Buffer Assembly. The *USE Processor Module* is used in place of the MEX6800 MPU Module in the EXORciser and provides the following functions:

- Shares its MC6800 MPU device between the EXORciser and the user's system.
- Provides the EXORciser internal clock circuitry.
- Provides the option of using the EXORciser clock within the EXORciser.
- Enables the overall system – user's system and EXORciser – to operate with the user's system clock.
- Interfaces the MC6800 MPU address, data, and control signals with the EXORciser bus.
- Interfaces the MC6800 MPU address, data, and control signals with the user's system via the USE Cable and Buffer Assembly.
- Interfaces selected MC6800 MPU signals ($\overline{IRQ}$, $\overline{NMI}$, HALT, VMA, and BA) with the optional Systems Analyzer Module via the USE Intercept Module.

The *USE Intercept Module* plugs directly into the EXORciser bus and is used to mount the optional Systems Analyzer Module. A cable assembly couples the selected control signals between the Systems Analyzer and the USE Processor Module.

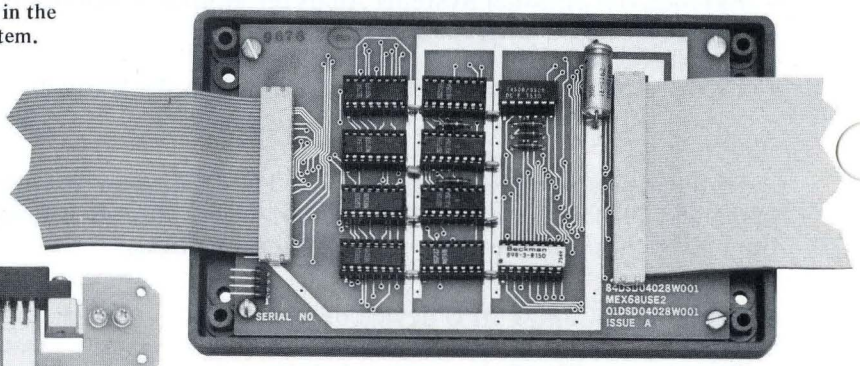
The *USE Cable and Buffer Assembly* connects the USE Processor Module into the user's system. A 40-pin connector on this assembly plugs into the MPU socket in the user's system permitting the USE Processor Module's MPU to control the operation of the user's system. In this application everything within the EXORciser appears to be within the MPU in the user's system. Through special jumper connections, this assembly also can transfer the timing signals required by the dynamic memories in the EXORciser to operate with the user's system clock. In addition, the USE Cable and Buffer Assembly buffers the transferred signals.

ISSUE A

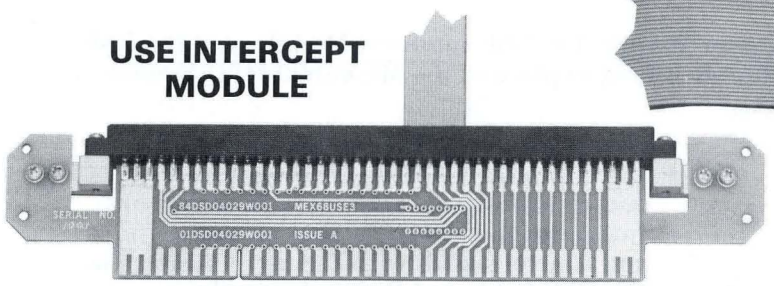
MEX68USE
User System Evaluator (USE)

Specifications

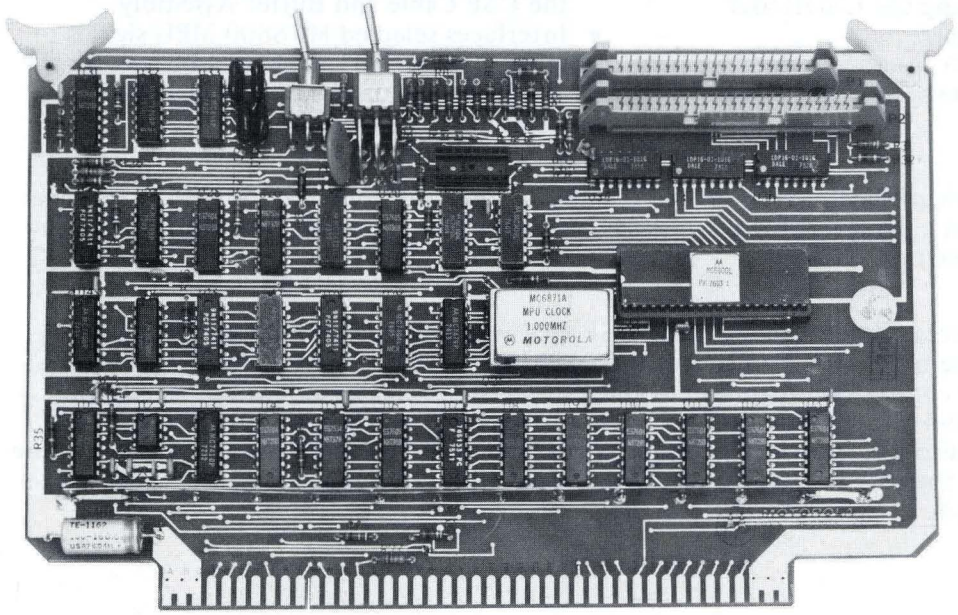
Microprocessor	MC6800 MPU
Word Size	
Data	8 bits
Address	16 bits
Instruction	8, 16, or 24 bits
Instruction Set	72 variable length instructions
Addressing Modes	Seven address modes – Direct, Relative, Immediate, Indexed, Extended, Implied, and Accumulator
Memory Size Capability	65,536 bytes with the EXORciser EXbug Firmware (when used) using 4K bytes. Addresses EXORciser ROM, RAM, and I/O and user's system ROM, RAM, and I/O in any combination.
Clock Signals	Switch Selectable Crystal controlled 1 MHz clock with capability to work with dynamic and slow memories. Operates in the EXORciser system. or User's system clock operating in the EXORciser and the User's system.
Operating Temperatures	0 to 70° C.
Power Requirements	+5 Vdc at 1.5 A
Physical Characteristics	
USE Processor Module	
Width	9.75 in.
Height	5.75 in. above connector
Board Thickness	0.062 in.
USE Intercept Module	
Width	9.75 in.
Height	1.875 in.
Board Thickness	0.062 in.
Cable Assembly Length	1 ft.
USE Cable and Buffer Assembly	
Case Height	0.875 in.
Case Length	7.50 in.
Case Width	4.32 in.
Cable Assembly Length	2 cables 5 ft. each 1 cable 13 in.



USE CABLE AND BUFFER ASSEMBLY (Cover Removed)



USE INTERCEPT MODULE



USE PROCESSOR MODULE

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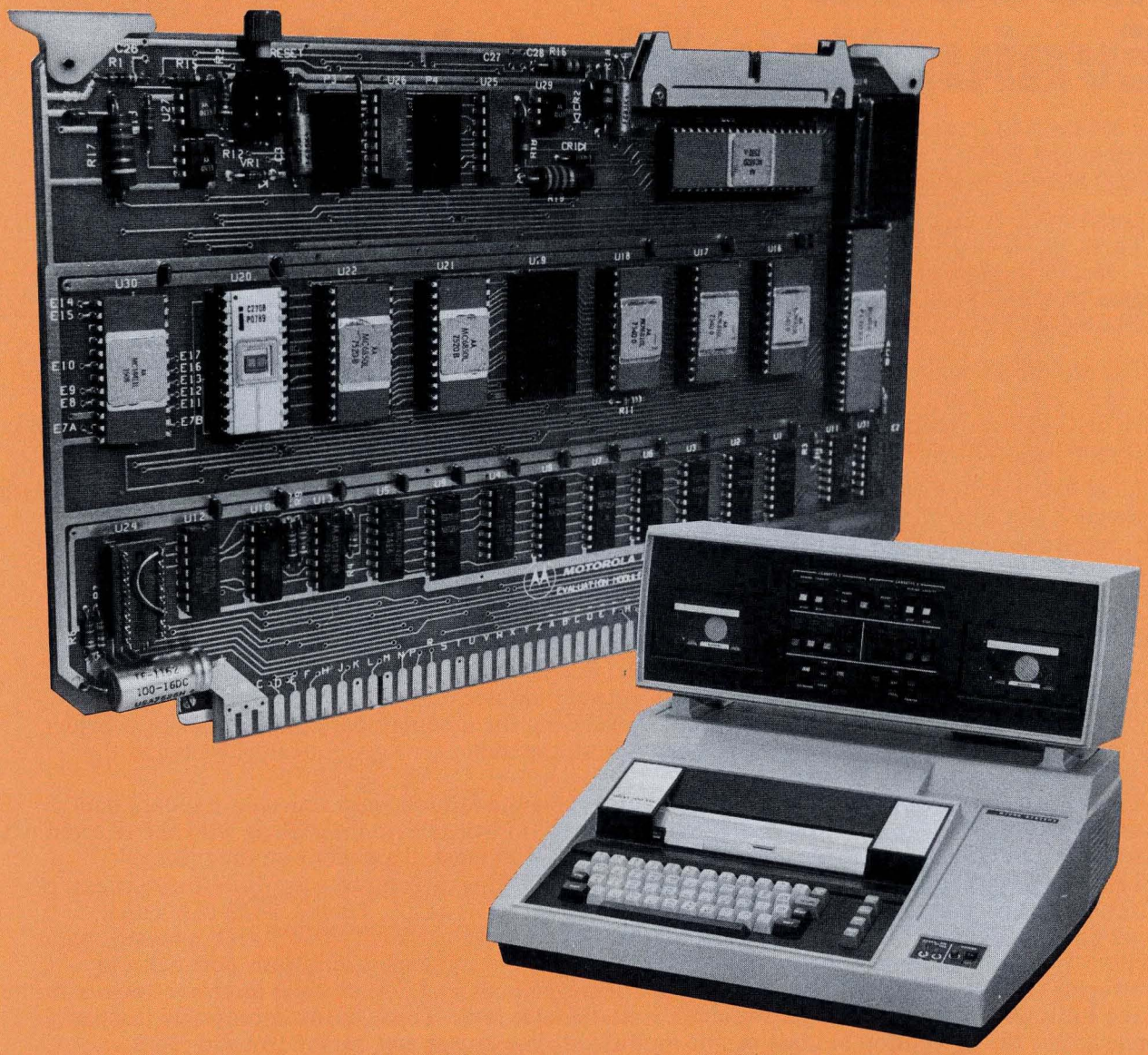

M6800B Evaluation Module II

For Hardware Evaluation and Program Development

ISSUE A

M6800B Evaluation Module II

The M6800B Evaluation Module II is a Microcomputer that provides the user with an efficient and economical off-the-shelf means to evaluate the operating characteristics of the M6800 Microcomputer family of parts in various applications. It contains the following components:

- One M6800 Microprocessing Unit (MPU)
- Three MCM6810 128 x 8 Random Access Memories (RAM)
- One MCM6820 Peripheral Interface Adapter (PIA)
- One MCM6830 1024 x 8 Read Only Memory (ROM)
- Two MC6850 Asynchronous Communciations Interface Adapters (ACIA)
- One MC14411 Bit Rate Generator (BRG)
- Data and address buffers

The M6800B Evaluation Module II interfaces with either a TTY (20 mA neutral current loop) or an RS-232C compatible terminal. This data terminal provides direct communication with the module's MINIBUG control program. The MINIBUG control program, stored in the module's read only memory, in conjunction with the selected data terminal, provides the following functions:

- Load data into the Evaluation Module
- Display and, if required, change the data in the module's random access memory
- Display and, if required, change the contents of the MPU registers
- Print out or punch (record) on tape the data stored in the module's memory
- Set the number of stop bits for data communication
- Run the user's program

The Evaluation Module provides the user with 256 bytes of random access memory on which to develop his programs. In addition, this module, through its address and data buffers, is capable of interfacing with additional memory and input/output modules.

The module's clock circuitry, in addition to generating the module's basic timing signals, provides the Evaluation Module with dynamic memory refresh capability on a cycle stealing basis and the ability to work with slow memories.

The MC14411 Bit Rate Generator provides the Evaluation Module with fourteen standard baud rates – six of which are jumper selectable. The MINIBUG II Firmware, in interfacing with the selected data terminal, is capable of transferring data at either 110 or 300 baud, dependent on the terminal.

The Evaluation Module also has the capability of connecting directly to a user's defined process or peripheral device through its MC6820 PIA and second MC6850 ACIA. The MC6820 PIA's dual input/output ports and control lines permit interfacing the Evaluation Module with keyboards, basic printers, displays, and similar devices. The MC6850 ACIA's serial communications port permits interfacing the Evaluation Module with modems, data terminals, and similar serial interface devices at one of the Bit Rate Generator's jumper selectable data transfer rates. Through the appropriate jumper connections, the Evaluation Module can be modified to operate at any one of 14 baud rates.

Options

Option	Part Number	Description
1	MEC6800B	Assembled and Tested Evaluation Module Assembly
2	MEC6800B1	Bareboard – Printed Circuit Board only. User supplies components.

Parts supplied with the MEC6800B – Three 16-pin component boards.
PIA Connector and Flatribbon Cable.
M6900B Evaluation Module II User's Guide.

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M6800B Evaluation Module II

Specifications

Power Requirements	+5 Vdc @ 2 A +12 Vdc @ 50 mA -12 Vdc @ 50 mA
Clock Frequency	921.6 kHz
Signal Characteristics	
Connector P1	
Address Bus	Three-State TTL Voltage Compatible
Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μA max at 2.6 V
Data Bus	TTL Voltage Compatible
Input Logic "0"	0.0-0.85 V (-200 μA max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μA max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Control Bus	
Input Logic "0"	TTL Voltage Compatible
Input Logic "1"	TTL Voltage Compatible
Output Logic "0"	0.5 V max at 40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Connector P2, PIA Signals	
Data Signals	
PA0-PA7 Input/Output Lines	TTL Voltage Compatible
PB0-PB7 Input/Output Lines	Three-State TTL Voltage Compatible
Control Lines	
CA1, CA2, and CB1	TTL Voltage Compatible
CB2	Three-State TTL Voltage Compatible
Connector P3, Terminal Interface Signals	
Data Transfer Rate	110 or 300 Baud
Data Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
Reader Control Signal	Control signal for manual TTY devices modified for external control
Connector P4, Terminal Interface Signals	
Data Transfer Rate	110, 134.5, 300, 600, 1200 and 2400 Baud (with jumper modifications 75, 150, 200, 1800, 3600, 4800, 7200 and 9600).
Data Signals	EIA RS-232C compatible

Connections and Descriptions

Connector P1 — Data, Address, and Control Bus

Signal Mnemonic	Signal Name and Description
$\overline{\text{IRQ}}$	$\overline{\text{Interrupt Request}}$ – This input signal requests that an interrupt sequence be generated within the MPU. The processor will wait until it completes the instruction that is being executed before it recognizes the request. Then, if the interrupt mask bit in the condition code register is not set (interrupt not masked), the MPU will begin an interrupt sequence. The MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur.
$\overline{\text{NMI}}$	$\overline{\text{Non-Maskable Interrupt}}$ – This input signal requests that a non-maskable interrupt sequence be generated within the processor. The processor will complete the instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal.
VMA	Valid Memory Address – This output indicates to the memory and peripheral devices that the address on the address bus is valid.
$\phi 2$	Phase 2 Clock signal – This signal is derived from the memory clock and used to synchronize the transfer of data on the data bus.
MEMCLK	Memory Clock – This is the basic 921.6 kHz clock signal used by the Evaluation Module to generate its $\phi 1$ and $\phi 2$ clock signals. A dynamic memory device would use this signal to control its timing.

Connections and Descriptions

Connector P1 — Data, Address, and Control Bus (continued)

Signal Mnemonic	Signal Name and Description
TSC	Three-State Control – This input, when high, causes all of the address lines and read/write line to go to their off, or high-impedance, state. The valid memory address, valid user's address, and the bus available signals will be forced low. The data bus is not affected by the three-state control.
BA	Bus Available – This output signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the Halt line is low or the MPU is in the WAIT state as the result of executing a WAIT instruction.
MEMRDY	Memory Ready – This signal enables the Evaluation Module to work with slow memories. The Evaluation Module, on receiving a low level Memory Ready input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 2$ high.
D0-D7	Data Bus – These bi-directional lines, when enabled, transfer data between the MPU and any external modules.
A0-A15	Address Bus – This address line, when enabled transfers the MPU program counter output to any external modules.
HALT	Halt – When this input is in the high state, the MPU will fetch the instruction addressed by the program counter and start execution. When low all activity in the MPU will be halted.
RESET	Reset – This line goes low when the RESET switch is actuated and may be used to reset any external devices. The RESET switch, on being actuated, initiates a MC6800 MPU cold-start vectored interrupt routine.
R/W	Read/Write – This MPU output signal indicates to the external modules whether the MPU is in a read (high) or a write (low) state. The normal standby state of this signal is read (high).
REFREQ	Refresh Request – This signal, when present, initiates a memory refresh operation. The Evaluation Module, on receiving this input from an external module, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 1$ high and, through the Refresh Grant command, instructs the dynamic memory modules to refresh their memories.
REFGNT	Refresh Grant – This signal instructs the dynamic memory modules to refresh their memories.
VUA	Valid User's Address – This signal indicates to the memory and peripheral devices that the address on the bus is valid. On Evaluation Module II, VUA is the same signal as VMA.

Connector P2 — Peripheral Interface Adapter Signals

Evaluation Module II provides the user with the capability of connecting a parallel peripheral device to the module's MC6820 PIA. This PIA has dual 8-bit input/output ports – PA0-PA7 and PB0-PB7 – along with four control lines – CA1, CA2, CB1, and CB2. Refer to the M6800 System Design Data for details on these signals.

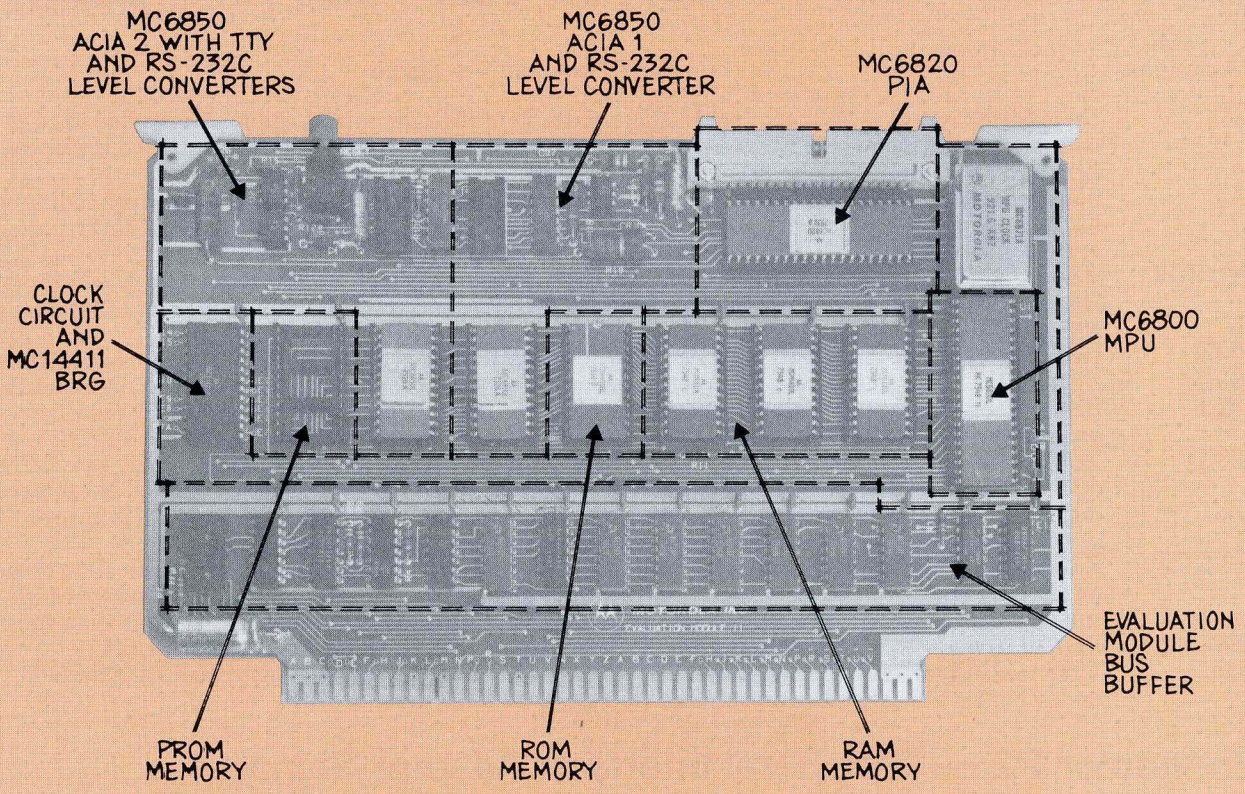
Connector P3 — TTY/RS-232C Terminal Interconnection Signals

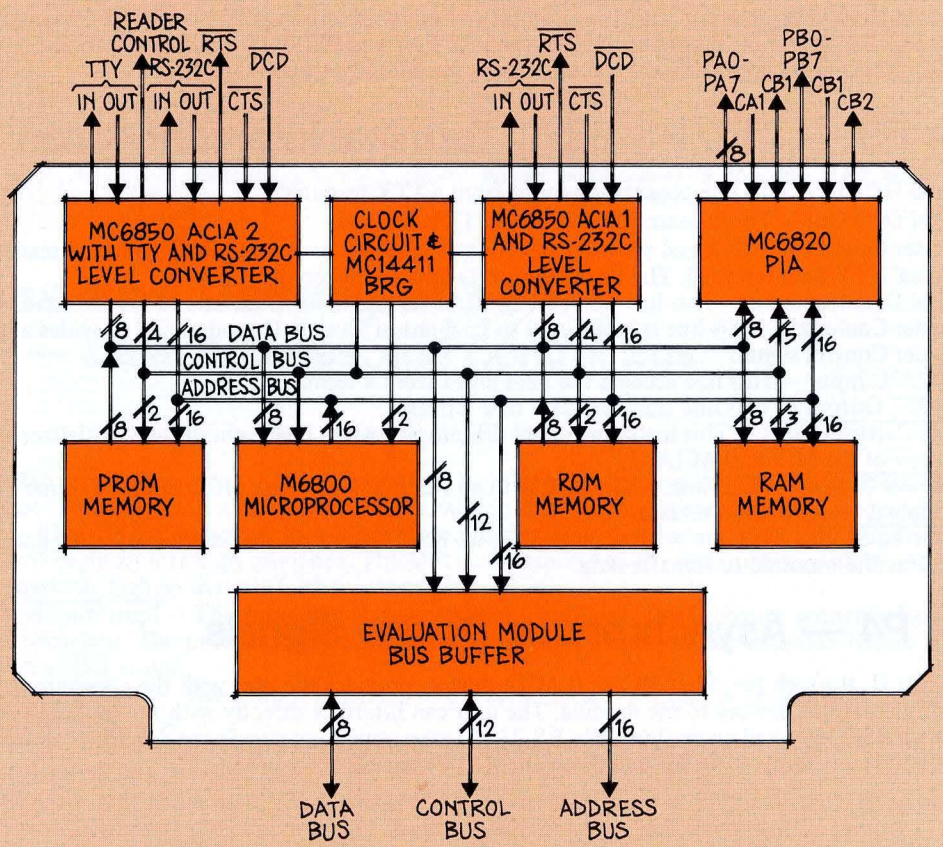
TTY IN	Serial Data In – This line accepts the input from a TTY terminal.
TTY OUT	Serial Data Out – This line transfers data to a TTY terminal.
–	Reader Control – This signal provides the control required to operate the paper tape reader on a modified manual TTY data terminal. The terminal now is under MPU control.
–	Serial Data Common – This line provides a return for the Serial Data In and Serial Data Out signals.
–	Reader Common – This line is connected to Evaluation Module II ground and provides a return for the Reader Control signal.
RS-232 IN	RS-232C Input – This line accepts the data input from a terminal.
RS-232 OUT	RS-232 Output – This line transfers data to a terminal.
DCD	Data Carrier Detect – This high impedance TTL input, when high, inhibits and initializes the receiver section of the MC6850 ACIA.
RTS	Request to Send – This line, when used with an RS-232C terminal, informs the terminal that Evaluation Module is ready to receive data.
CTS	Clear To Send – This line is a low level when an RS-232C terminal is connected to Evaluation Module II and informs the terminal to transfer data.

Connector P4 — Asynchronous Device Signals

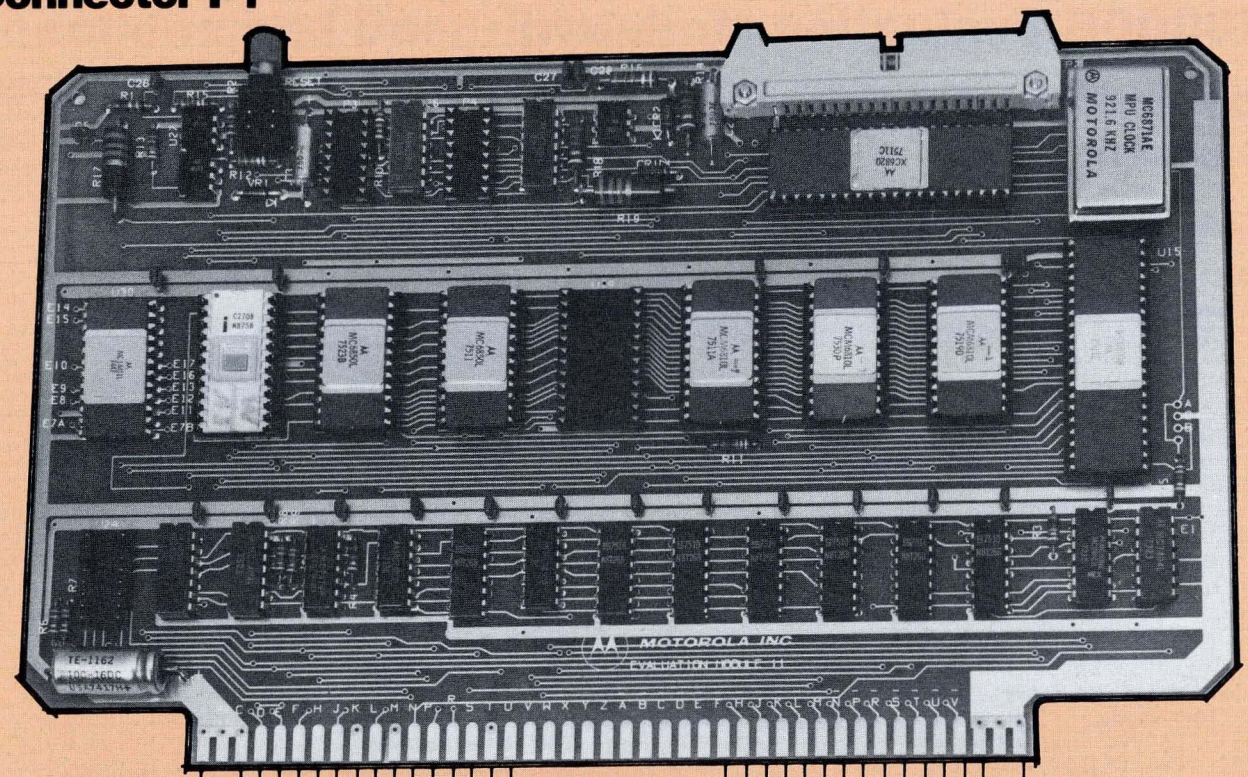
Evaluation Module II, through the other MC6850 ACIA device, provides the user with the capability of connecting asynchronous communications devices to the module. The user can interface directly with the module's ACIA or through the module's RS-232C level converters. The RS-232C interconnection signals are described above. Refer to the M6800 System Design Data for details on the ACIA's signals.

Evaluation Module II



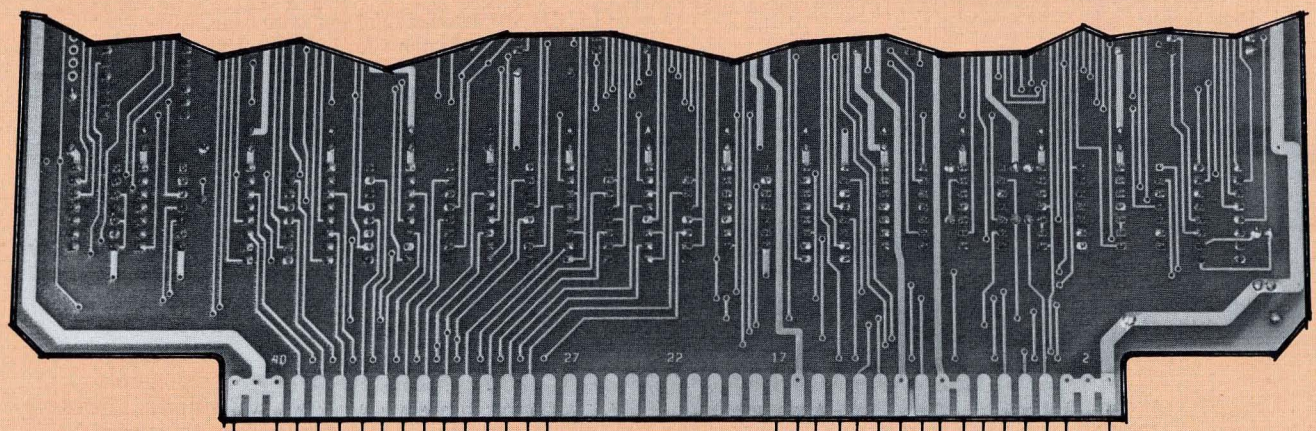


Connector P1



+5VDC
IRQ
NMI
VMA
GND
ø2
GND
MEMCLK
-12VDC
TSC
BA
MEMRDY
NOT USED
+12VDC
NOT USED
D3
D7
D2
D6
A14
A13
GND
A1
A2
A5
A6
A9
A10

FRONT VIEW



GND
A0
A3
A4
A7
A8
A11
A12
A15
D4
D0
D5
D1
NOT USED
-12VDC
REFREQ
REFGNT
NOT USED
+12VDC
VUA
+5VDC
HALT
RESET
R/W
NOT USED
GND

REAR VIEW

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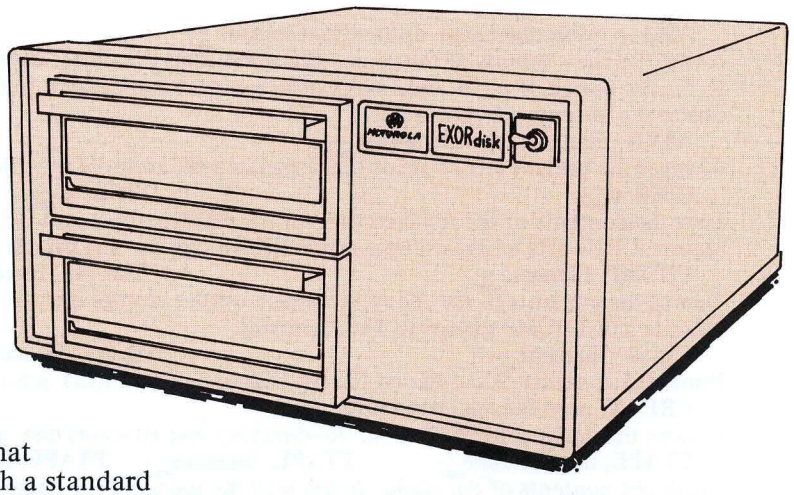
MOTOROLA MICROSYSTEMS

The only peripheral required to use the EXORciser for design purposes is a data terminal. For major design efforts, however, considerable design time can be saved with additional peripherals that speed up program development. EXORdisk and EXORtape are among these development tools.

M6800 Support Peripherals

MOTOROLA MICROSYSTEMS

M6800 EXORdisk



The EXORdisk is a "floppy disk" storage system that extends the EXORciser capacity by up to one-million bytes of memory. Together with the EXORciser, and a separately available Interface Module, it provides a complete program-development system whose high-speed capabilities can be matched only by much more expensive minicomputers. The floppy disk system allows the user to assemble, in 30 seconds, programs that would require up to 2½ hour assembly time with a standard ASR-33 teletype reader.

The EXORdisk system consists of the disk-drive mechanism and a diskette which houses the EXORciser Flexible Disk Operating System II, EDOS II. The latter controls the EXORdisk and interface operations. Functions include the loading of data from the EXORdisk to the EXORciser memory or different diskettes and between diskettes and other storage media such as paper tape and cassette. If desired, the EDOS II program may be purchased on a separate diskette which contains, in addition, the M6800 Resident Editor and Assembler programs. This permits disk-to-disk program editing and assembling in addition to the various transfer functions.

The EXORdisk connects to the EXORciser via an interface module that is an optional component of the EXORciser. This module can be used to simultaneously connect an EXORtape peripheral to the EXORciser.

The EDOS II program will handle and control up to four disk drives, thereby offering memory capacity ranging from 256,256 eight-bit bytes to over 1-million bytes.

Specifications

Diskette Format:
- 2,050,048 Bits/Diskette
- 256,256 Bytes/Diskette
- 77 Tracks/Diskette
- 26 Sectors/Track
- 128 Bytes/Sector

Performance:
- Rotational Speed – 360 RPM
- Track-To-Track Access Time – 10 ms
- Head Load – 40 ms
- Sector Read/Write Time – 5 ms
- Average Latency Time – 83 ms
- Interrecord Time – 1 ms
- Head Unload Time Out – 700 ms (for maximum head and media life)

Power Requirements: 115/220 Vac, 50/60 Hz, 200 Watts

Physical Characteristics: (2-drive system)
- L x H x D 17 x 8 3/4 x 17 inches
- Weight 65 pounds

Electrical:
- All signals are TTL, Low-True
- 16 Output Lines, 8 Input Lines

Options and Ordering Information

Part Number	Description
M68FD3602	EXORdisk with two drives (includes appropriate two-drive cable)
M68FD3602-12	EXORdisk for 220 V, 50/60 Hz operation
M68FD3602-19	19-inch rack mounting kit
M68FD3602-24	Cable for expanding from two-drive to four-drive system.
M68IFC	M6800 EXORciser Interface Module
M68XAE6812D	Diskette containing EDOS II, M6800 Resident Editor and M6800 Resident Assembler

ISSUE A

EXORdisk Commands

ASM, p, sourcefilename, destinationfilename↵
Assembles the contents of the source file and directs the object to the destination file. If p = 3, only a listing is generated to the list device. If p = 4, only a hex object output is generated to the output object file. If p = 2, both listing and object file outputs are generated.

ATTR, filename, newattributes↵
Changes the present attributes of the designated file to those specified in the new attributes field.

CDIR:u↵ **PDIR: u**↵
Lists the contents of the file directory on the diskette drive unit 0-3. Lists the filenames, attributes, and file size in sectors. CDIR lists on the console and PDIR lists on the line printer.

CDUMP, filename↵ **TDUMP, filename**↵
Dumps the contents of the file to the punch output storage device or the communication link device. CDUMP dumps to cassette and TDUMP dumps to TTY terminal.

CLIST, filename↵ **PLIST, filename**↵
Prints the contents of the file on the list output device. CLIST prints on the console and PLIST prints on the line printer.

CREAT, newfilename, newfilesize↵
Creates the designated filename in the directory and allocates disk space equal to the size.

CTAPE, newfilename↵ **TTAPE, filename**↵ **PTAPE, filename**↵
Loads the contents of the reader device into the specified file name on diskette. CTAPE transfers from cassette, PTAPE transfers from a high speed paper tape reader, and TTAPE transfers from a TTY terminal.

CXGEN↵ **PXGEN**↵ **TXGEN**↵
Enables system generation of other EDOS versions that may become available in the future.

DUP↵
Copies the contents of the diskette in drive unit 0 onto the diskette in drive unit 1.

EDIT, inputfilename, newoutputfilename↵ **EDIT, newoutputfilename**↵
Enables editing of the input file's contents. Edited data is stored into the output file.

EXBUG↵
Returns to the EXORciser EXbug control program.

HOME: u↵
Positions the disk head on drive unit u (0-3) to track 0.

INIT: u↵ **INITX**↵
Initiates the file directory on the diskette in drive unit u. Clears any existing user files on the diskette. INITX implies drive unit 0 and u in INIT: u designates drive unit 1, 2, or 3.

LOAD, objectfilename↵
Loads the contents of the file into RAM memory for execution.

MERGE, newfilename, filename1, filename2. . . filenamen↵
Creates a new file which is a concentration of filenames 1-n, in that order.

PURGE: u, filename1, filename2. . . filenamen↵
Deletes the designated files from the diskette in drive unit u (0-3) and then repacks the contents of that diskette, making disk space available for additional files.

RENAM, oldfilename, newfilename↵
Renames the old file with the new file name.

Interface Command and Data Words
all signals are compatible with MC6820 PIA Chips

Input Data and Status: 8 bits, negative true, PIA address ECOO, bits 0-7
Logic 1: 0 to 0.4 volts
Logic 0: 2.4 volts min

Note: IRQA1 bit 7 is device BUSY.

Output Data: 8 bits, negative true, PIA address ECO6, bits 0-7.

Output Commands: 8 bits, negative true, PIA address ECO2, bits 0-7.

COMMAND FUNCTIONS

SEEK AND VERIFY: Seeks Selected Track and Verifies Track Address from ID Field:

SEEK TRACK 0: Seeks Track 0

SECTOR AND UNIT SELECT: Specifies Sector and Unit Number for Read/Write Operation

TRACK SELECT: Specifies Selected Track to be used by Next Seek

WRITE: Write Contents of Write Buffer to Selected Sector and Unit on existing track

READ: Reads Contents of Selected Sector into Read Buffer

WRITE DELETED DATA ADDRESS MARK: Same as Write but uses header in Data Field which can later be detected in Read Operation

READ CRC: Same as Read but no data is transferred to the Read Buffer. Used to verify integrity of data previously written

SHIFT WRITE BUFFER: Loads Data into Write Buffer

SHIFT READ BUFFER: Inputs Data from Read Buffer

GATE STATUS: Gates Status or Data onto Input Data Lines.

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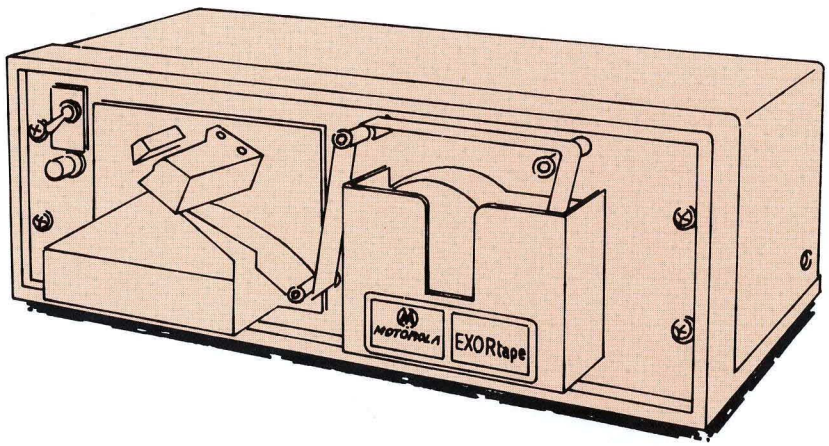
MOTOROLA MICROSYSTEMS

M6800 EXORtape

- Plug Compatible with the EXORciser
- Compatible with the EXORciser's EXbug Firmware and Resident Software
- Up to 25 Times Faster Than a Standard ASR-33 Teletype Reader
- Photo Electric Character Detector for More Reliable Loading
- Derated Long Life, Line Filament Type Lamp



EXORtape is a high-speed paper-tape reader that provides an efficient means for program loading, editing and assembling. It is capable of loading up to 250 characters per second into EXORciser memory. The EXORtape connects to the EXORciser through the optional M6800 EXORciser Interface Module and is completely compatible with the EXORciser EXbug firmware and the M6800 Resident Software. Its Interface program also permits the user to daisey-chain other peripherals, such as the EXORdisk, into the system.

Specifications

Electrical	
Input Data	8 bits
Status Input	Reader busy
Start Command	HPST start bit
Power Requirements	115 Vac, 60 Hz single phase, 40 W
Optional	220 Vac, 50/60 Hz single phase
Manual Advance	Front panel push button
Speed	Up to 250 characters per second
Physical	
Cables	One 40 line ribbon cable, length 5 feet
Dimensions L x H x D	17-½ x 6 x 8-½"
Mounting	Stand alone, rubber feet, optimal 19 inch RETMA rack mount
Weight	10 pounds
I/O Cabling	Rear/Center
Tape Holder	Up to 5 inches diameter tapes

Options and Ordering Information

Part Number	Description
M68R680	Table Top EXORtape
M68R680-12	EXORtape with 220, 50/60 Hz Power Requirement
M68R680-19	19-inch Rack Mounting EXORtape
M68IFC	M6800 EXORciser Interface Module

ISSUE A